EORGIA INSTITUTE OF TECHNOLOGY — OFFICE OF CONTRACT ADMINISTRATION

PROJECT ADMINISTRATION DATA SHEET

[X] ORIGINAL [ ] REVISION NO. ____

Project No. A-3183 DATE 3-24-82

Project Director: ~~D. K.~~ Tibbitts Co ~~School~~/Lab SEL

Sponsor: Comptek Research, Inc, One Technology Center 45 Oak Street, Buffalo, N.Y. 14203

Type Agreement: Letter Subcontract No. BED 21121

Award Period: From 3-5-82 To ~~3-31-82~~ (Performance) ~~3-31-82~~ (Reports)

Sponsor Amount: $ 10,000 ~~4-30-82~~ 6/30/83 5/30/82 Contracted through:

Cost Sharing: None ~~5/30/82~~ 3/1/84 GTRI/~~GIT~~

Title: Development of EEPROM Adapter

ADMINISTRATIVE DATA OCA Contact Don Hasty

1) Sponsor Technical Contact:

Mr Steve Cooper
Comptek Research, Inc
One Technology Center
45 Oak Street
Buffalo, N.Y. 14203
(716) 842-2700

2) Sponsor Admin/Contractual Matters:

Mr Thomas Ciaccia
Contracts Administrator
Comptek Research, Inc
One Technology Center
45 Oak Street
Buffalo, N.Y. 14203
(716) 842-2700

Defense Priority Rating: N/A Security Classification: N/A

RESTRICTIONS

See Attached DOD Supplemental Information Sheet for Additional Requirements.

Travel: Foreign travel must have prior approval — Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

Equipment: Title vests with N/A - None proposed

COMMENTS:

COPIES TO: Res Admin Network

~~Administrative Coordinator~~
Research Property Management
Accounting
Procurement/EES Supply Services
Research Security Services
~~Reports Coordinator (OCA)~~
Legal Services (OCA)
Library
EES Public Relations (2)
Computer Input
Project File
Other ____

FORM OCA 4-781

EORGIA INSTITUTE OF TECHNOLOGY — OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION/CLOSEOUT SHEET

Date 8/23/85

roject No. A-3183 — ~~School~~Lab SEL

ncludes Subproject No.(s)

roject Director(s) T. Tibbitts — GTRC ~~XXX~~

ponsor Compt~~ex~~ek Research Inc. Under Prime F09650-82-C-0140

itle Development of EEPROM Adapter

ffective Completion Date: 6/30/83 (Performance) 6/30/83 (Reports)

rant/Contract Closeout Actions Remaining:

- [X] None
- [ ] Final Invoice or Final Fiscal Report — Per GTRC, H. Rodgers, - Zero balance in Account 8/23/85.
- [ ] Closing Documents
- [ ] Final Report of Inventions
- [ ] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other

ontinues Project No. — Continued by Project No.

OPIES TO:

roject Director
esearch Administrative Network
esearch Property Management
ccounting
rocurement/GTRI Supply Services
esearch Security Services
eports Coordinator (OCA)
egal Services

Library
GTRC
Research Communications (2)
Project File
Other A. Jones; M. Heyser

FORM OCA 89.285

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

30 March 1982

COMPTEK Research, Incorporated
One Technology Center
45 Oak Street
Buffalo, New York 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject subcontract for the period 1 March 1982 to 31 March 1982 is presented herein.

The intent of this program is to design, build, and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

The first technical task of the month was the analysis of the Data Extraction Interface to determine its usefulness with an EEPROM CPU. Because of the time required for the extraction process, it was determined that the current DX board will not be suitable for use with the new CPU. The complete DX report is attached.

The second task was to review the Control Panel/Octal Display information supplied by COMPTEK and return our comments. These comments were returned by phone on 25 March to Don Liedke and a copy of these comments is attached. During the same call, COMPTEK indicated that two boards were preferable for the master/slave adapters as opposed to a single card containing both circuits. Also, COMPTEK was informed of an error on the EEPROM CPU schematics; J3 pins 2, 4, 6, 8, 10, and 12 should be tied to ground but are not shown on the schematic.

The basic design (block diagram/signal flow level) has been started and should be completed before the preliminary design review.

Problem Areas

Georgia Tech EES has suggested that COMPTEK look into placing RAM on the adapter card. This should be resolved as quickly as possible to avoid delaying the design effort.

It appears that the DX card will at least be modified if not completely redesigned. This is to be done by COMPTEK but Georgia Tech EES will need to know as soon as possible if this mod/redesign will affect the adapter design.

Summary of Project Meetings

The orientation design review was held on 11 and 12 March at the Georgia Tech EES Cobb County Facility. Attached is a copy of the approved minutes.

Summary of Cost Incurred

The following costs were incurred:

Direct Salaries	$ 1,432.05
Retirement	161.46
Travel	-0-
Materials & Supplies	11.82
Overhead (55%)	882.93
TOTAL	$ 2,488.26

Attached is a projected and actual expenditure plot.

Expected Technical Activities

The primary thrust during April will be to complete the basic design and to supply engineering support to COMPTEK in their effort to manufacture an EEPROM CPU.

Respectfully submitted,

[redacted]

Terry Tibbitts
Project Director

TET/dta
Attachment

APPROVED:

[redacted]

David K. Plummer, Head
Surveillance Technology Branch

DATA EXTRACTION SYSTEM
DETAILED ANALYSIS

Prepared by
GEORGIA INSTITUTE OF TECHNOLOGY
ENGINEERING EXPERIMENT STATION

Prepared for
COMPTEK RESEARCH, INC.
One Technology Center
45 Oak Street
Buffalo, NY 14203

TABLE OF CONTENTS

TABLE OF FIGURES

1.0 INTRODUCTION AND GENERAL INFORMATION

1.1 Purpose

This report provides a detailed technical analysis of the ALR-46 ISS Data Extraction (DX) Interface and DR11-B Direct Memory Access Card to determine their usefulness with an ALR-46/-46A/-69 containing an EEPROM/Fairchild 9445 based CPU. The DX technical descriptions contained in this report are based on documentation provided by COMPTEK Research, Inc. This report was prepared under Subcontract Number BED 21121 for COMPTEK Research, Inc.

1.2 Description

The current DX Interface card was developed to be used with the ROLM 1601 and DVP 25 CPU processors. Recently however, a new CPU has been designed for the ALR-46/-46A/-69 Radar Warning Receivers. This new CPU was designed around the Fairchild 9445 and utilized EPPROM and PAL technology. The instruction set of the 9445 microprocessor is a superset of the ROLM 1601 and DVP 25 and is therefore software compatible (with a few minor exceptions) with the older CPU designs.

Even though the new CPU is software compatible with the old CPU designs, the hardware is completely different. Only the I/O network (Data Bus, Device Select Bus, and I/O Control Bus) has remained intact. The speed of execution of the new CPU has also been greatly increased. Many of the hardware differences can be taken care of in the EEPROM CPU Adapter Interface, but others (primarily speed) have a direct impact on the DX Interface and must be discussed here. The DR11-B DMA Interface must also be examined for possible problems introduced by the new CPU.

1.3 Reference

The reader should be familiar with "DX Interface Technical Manual", COMPTEK Research, Inc., 17 February 1982 before reading this document. A copy of COMPTEK Drawing Number 04L026000 "Interface, DX" is also useful in understanding this report.

2.0 IMPACT OF 9445 CPU ON DX INTERFACE

2.1 Bus Structure

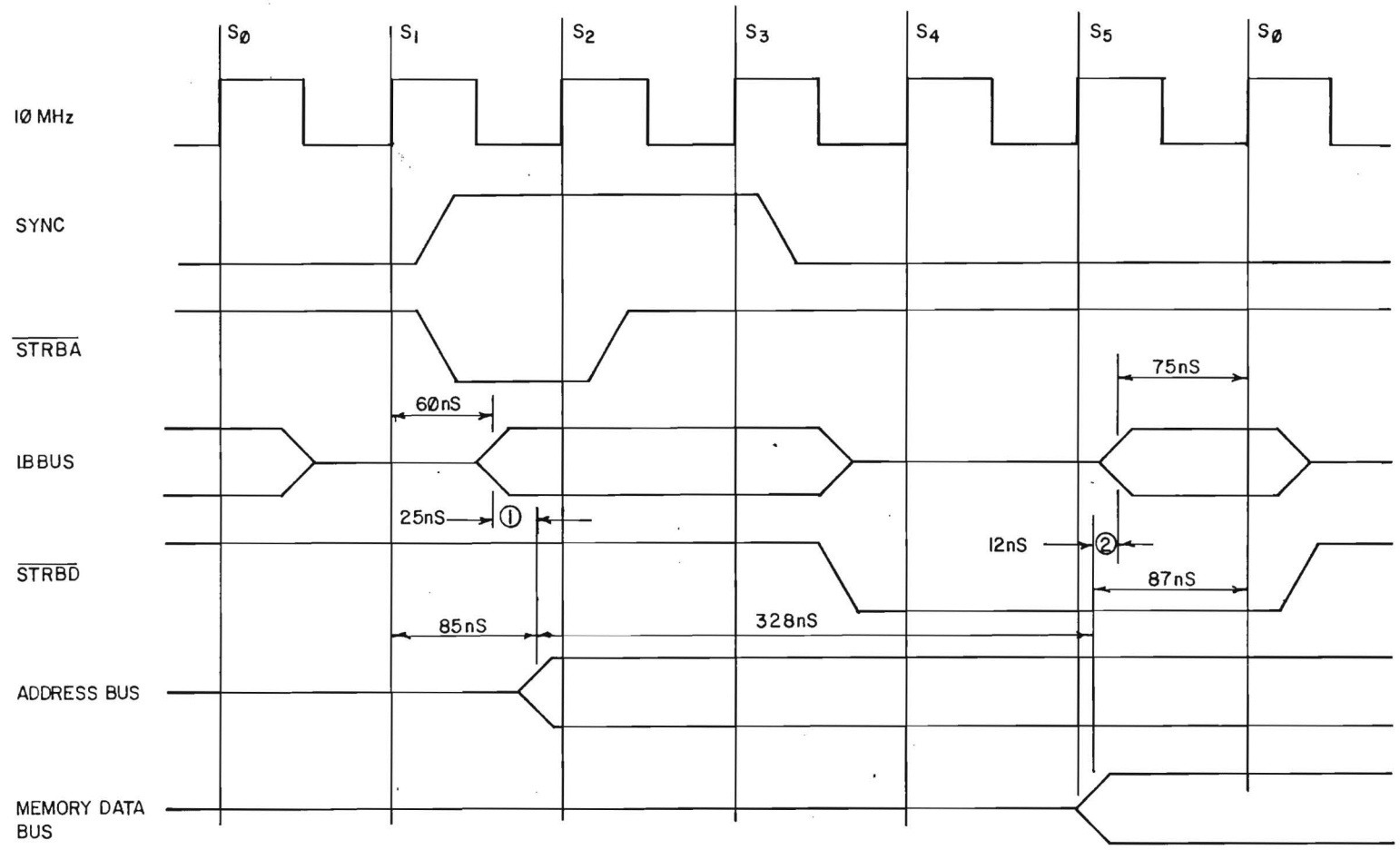
The DX Interface operates with the NOVA 3 type memory bus structure. This structure has a 15 bit address bus, a separate 16 bit data bus, and several control lines. The 9445 has a multiplexed 16 bit Information Bus (IB) and a different set of control lines. One of the tasks assigned to the EEPROM CPU Adapter Interface is to transform the 9445 control lines and IB bus into the DX Interface memory bus structure. At this time, no problems are seen in this area.

2.2 CPU Speed

Figure 1 shows the critical timing constraints for the 9445. This timing diagram assumes a 9445 running at 10 MHz, with no externally imposed wait states. A similar timing diagram for a 20 MHz system operating with externally imposed wait states (to utilize 300 ns EEPROM) would produce a similar cycle time. The overall cycle time for a write cycle is the same as that for a read cycle; some of the internal times change slightly.

The 9445 has a memory pre-fetch which allows it to process the current instruction while reading the next instruction from memory. Therefore, if the current instruction does not require a jump, indirect address calculation, or I/O operation, the next instruction can be executed 600 ns later. This means that the DX card must be able to process a new target address every 600 ns.

AF 23274



NOTES:

① WORST CASE PROPAGATION DELAY OF TRANSPARENT ADDRESS LATCH

② WORST CASE PROPAGATION DELAY OF MEMORY BUFFER

NO.	DESCRIPTION OF CHANGE	CH.	DATE

ENGINEERING EXPERIMENT STATION
OF THE
GEORGIA INSTITUTE OF TECHNOLOGY
ATLANTA, GEORGIA

TIMING CHART—
MEMORY READ FOR 9445 AT 10 MHz

SCALE: N.T.S.	DATE: 3/23/82
CONTRACT NO. BED 21/21	
PROJECT NO. A3183-000	

DR. COLEE
ENGR. T. E. T.
CH.
APP.

DRAWING NO.
A3183-001-A 2

K+E DE 7382 19-1253

3

3.0 DETAILED ANALYSIS OF DX INTERFACE

3.1 Bus Structure

As mentioned in Section 2, the EEPROM CPU Adapter will transpose the 9445 signals into those required by the DX Interface.

3.2 Bit Map Write Operation

The loading of the bit map is handled entirely by the DR11-B and will therefore not be affected by the new EEPROM CPU.

3.3 Bit Map Operation During Data Extraction

$\overline{\text{BWRITE}}$ and $\overline{\text{LTCHDAT}}$ will be much shorter in duration with the EEPROM CPU than with the older design. Figure 2 is a timing diagram of the expected read/write cycle signals produced by the EEPROM CPU Adapter Logic. Figure 3 is a timing diagram of the bit map operation with the expected adapter signals. No timing constraints are violated and the bit map should therefore operate properly with the new CPU.

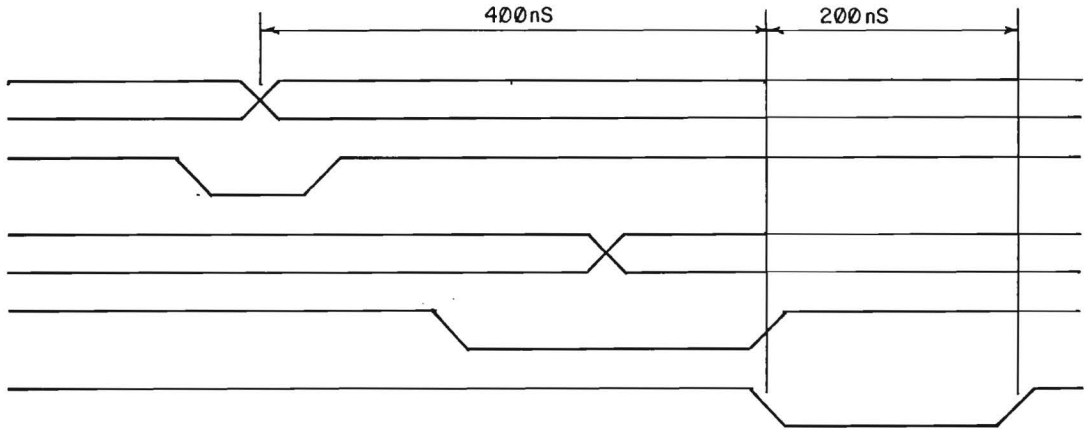
3.4 Write Sequence Controller

The Write Sequence Controller is a state machine which controls the loading of the FIFO buffer each time a "location" or "event" occurs. This state machine must operate fast enough so that two adjacent "locations" or "events" are loaded into the FIFO without fail. Figure 4 is a timing diagram of the location cycle. This cycle is triggered by U93A and U81 whenever a target memory location is modified. As shown, the earliest a new cycle (event or location) can begin is about 1.4μs from the time the memory write occurs. Figure 5 is a timing diagram for the event cycle. This cycle is triggered by U93B and U81 whenever a target memory location is read. In this case, the earliest a new cycle (event or location) can begin is 2.2μs.

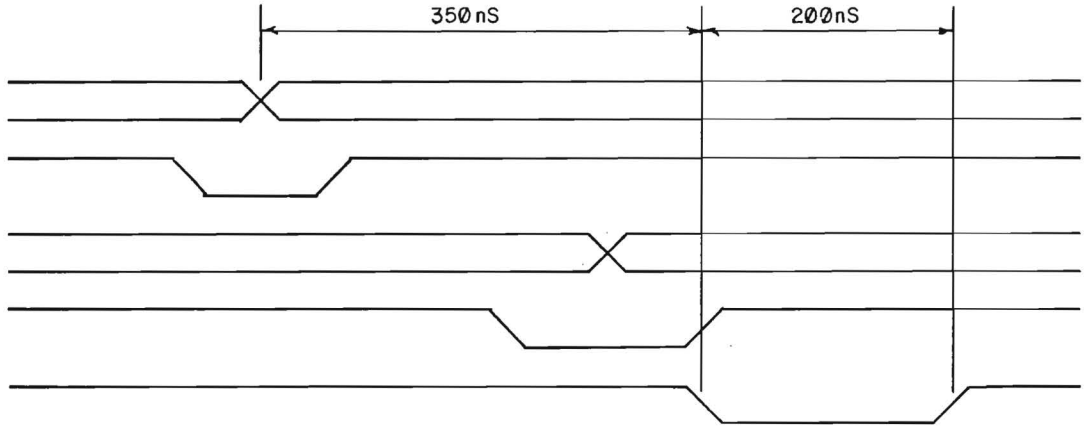
As pointed out in Section 2, the 9445 is running at a minimum cycle time of 600 ns. This means that after an arbitrary event or location occurrence, the DX Interface must be able to completely recover and be ready for the next trigger in less than 600 ns if it is to catch two adjacent triggers. The current DX Interface is not capable of meeting this requirement.

AF 23274

READ CYCLE



WRITE CYCLE



NOTE:

(1) THESE SIGNALS ARE NOT PRESENT ON DX, THEY ARE FOR INFORMATION ONLY.

NO.	DESCRIPTION OF CHANGE	CH.	DATE

SCALE: N.T.S. DATE: 3/23/82

CONTRACT NO. BED 21/21

PROJECT NO. A3183-000

ENGINEERING EXPERIMENT STATION
OF THE
GEORGIA INSTITUTE OF TECHNOLOGY
ATLANTA, GEORGIA

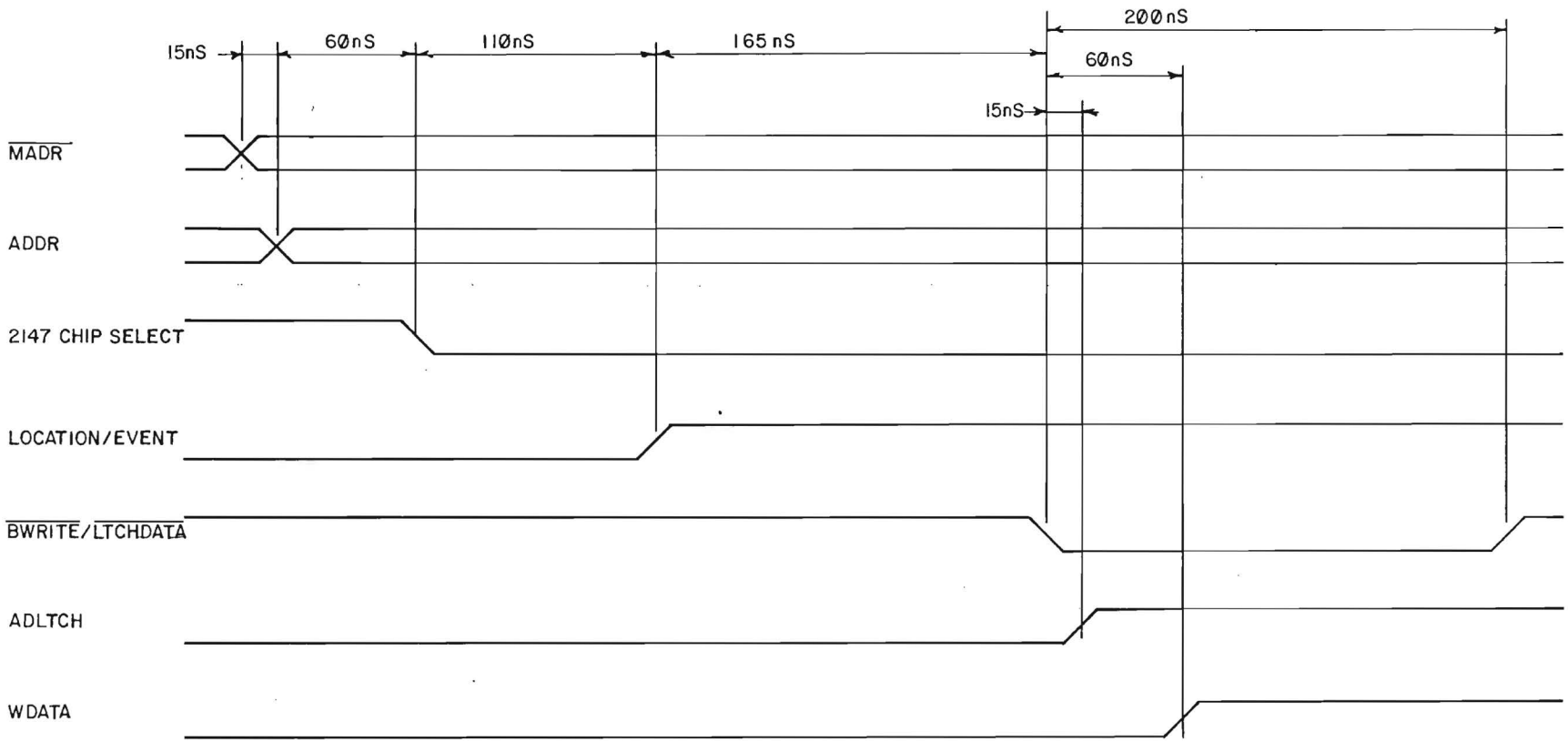
TIMING CHARTS-
PRODUCED BY EEPROM
ADAPTER

DR. COLEE
ENGR. T.E.T.
CH.
APP.

DRAWING NO.
A3183-002-A2

5

K+E DE 7342 19-1253



NO.	DESCRIPTION OF CHANGE	CH.	DATE

ENGINEERING EXPERIMENT STATION
OF THE
GEORGIA INSTITUTE OF TECHNOLOGY
ATLANTA, GEORGIA

TIMING CHART–
BIT MAP OPERATION WITH
EEPROM CPU

SCALE: N.T.S. DATE: 3/23/82

CONTRACT NO. BED 21/21

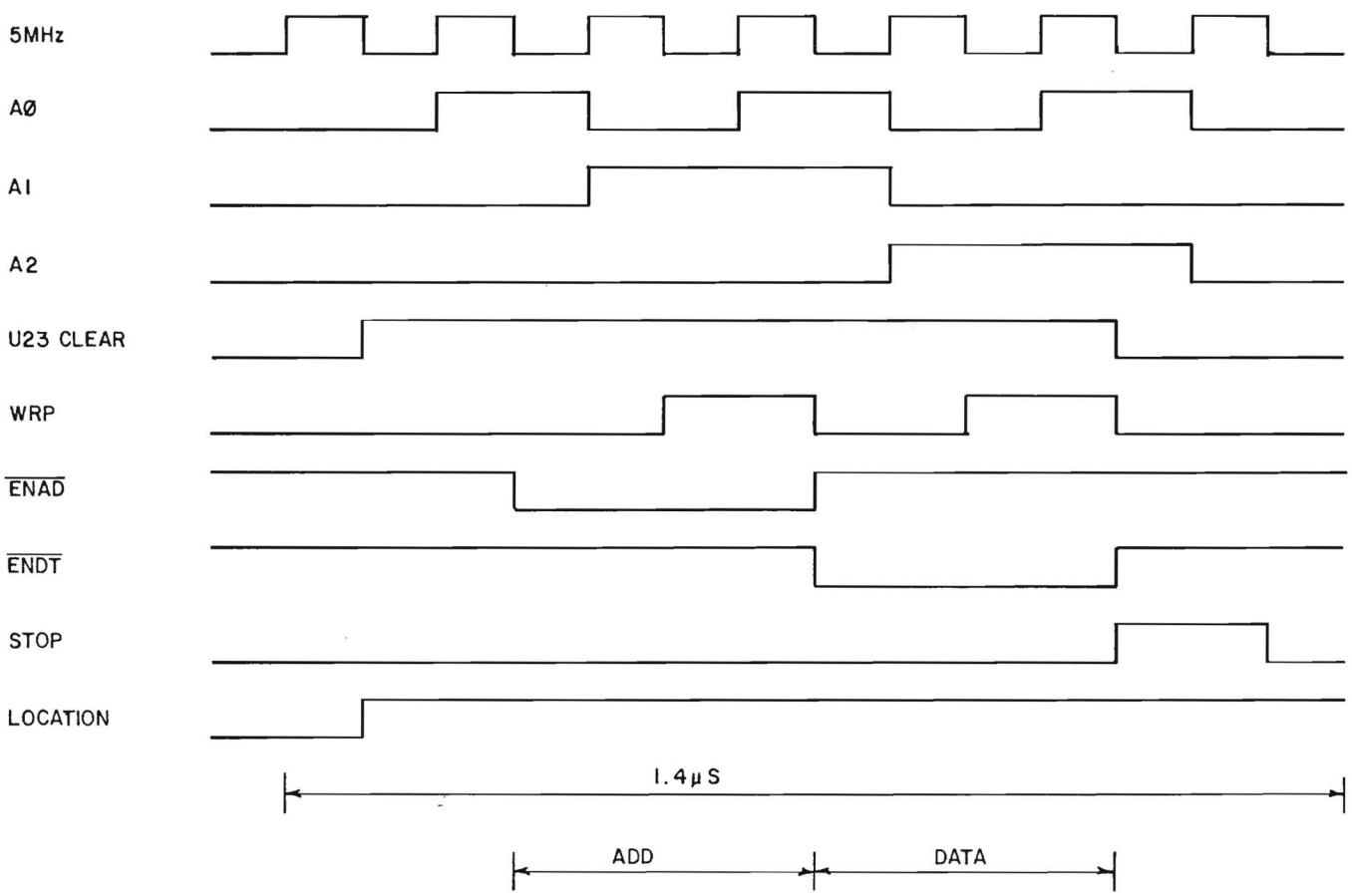
PROJECT NO. A3183-000

DR. COLEE
ENGR. T.E.T.
CH.
APP.

DRAWING NO. A3183-003-A 2

K+E DE 7382 19-1253

AF 23274



NO.	DESCRIPTION OF CHANGE	CH.	DATE

ENGINEERING EXPERIMENT STATION
OF THE
GEORGIA INSTITUTE OF TECHNOLOGY
ATLANTA, GEORGIA

TIMING CHART–
LOCATION

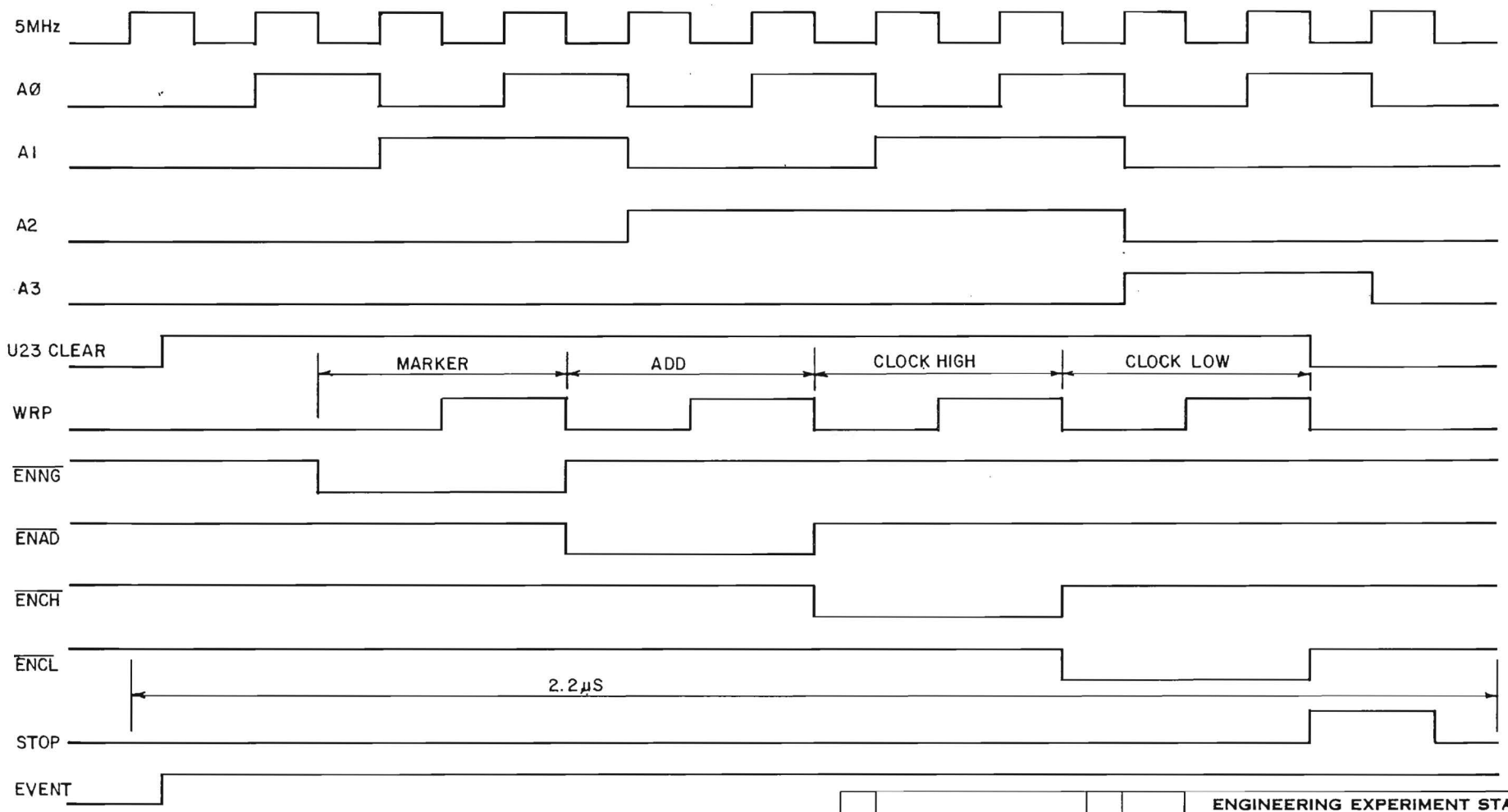
SCALE: N.T.S	DATE: 3/23/82
CONTRACT NO. BED 21/21	
PROJECT NO. A3183-000	

DR. COLEE
ENGR. T.E.T.
CH.
APP.

DRAWING NO.
A3183-004-A2

K+E DE 7362
19-1253

AF 23274



NO.	DESCRIPTION OF CHANGE	CH.	DATE

SCALE: N.T.S. DATE: 3/30/82

CONTRACT NO. BED21/21

PROJECT NO. A3183-000

ENGINEERING EXPERIMENT STATION
OF THE
GEORGIA INSTITUTE OF TECHNOLOGY
ATLANTA, GEORGIA

TIMING CHART-
EVENT

DR. COLEE
ENGR. J.E.T.
CH.
APP.

DRAWING NO.
A3183-005-A2

K+E DE 7362 19-1253

3.5 FIFO Buffer and DR11-B

The size of the FIFO buffer and the speed of the DR11-B Direct Memory Access (DMA) Interface to the host computer determines the number of consecutive triggers (events or locations) which can be accepted by the DX Interface. A buffer overflow will cause data loss during the extraction process.

A "location" trigger causes 2 words to be stored in the FIFO buffer; Address and Data. An "event" trigger causes 4 words to be stored in the FIFO buffer; -1, Address, Clock High, Clock Low. As pointed out in Section 2, an "event" can occur every 600 ns. This translates into 6,666,667 (1 ÷ 600 ns X 4) 16 bit words which must be transferred across the DR11-B to guarantee that the FIFO (no matter how large) will never overflow. The DR11-B can only transfer 500,000 words per second at best (less than 10% as fast as needed) which means the DX Interface will never be able to continuously extract every event in real time. That is, there is always an upper limit on the number of consecutive (adjacent) events which can be extracted.

From a practical standpoint, the size of the FIFO buffer will determine the number of adjacent events which may be captured and the average time between events to prevent overflow. If the FIFO were increased to 128 words, 35 consecutive events (at 600 ns/event) will cause overflow. The average time between events can never exceed 8μs (this is about 1 in 13 instructions) or the buffer will overflow regardless of how large the buffer is made.

4.0 RESULTS AND CONCLUSIONS

4.1 Bus Structure

The bus structure presents no unsolvable interface problems between the EEPROM CPU and the DX Interface.

4.2 Bit Map Write Operation

The current methods used to initialize the bit map are not affected by the new CPU.

4.3 Bit Map Operation During Data Extraction

The bit map itself is fast enough to operate with the proposed new EEPROM CPU adapter.

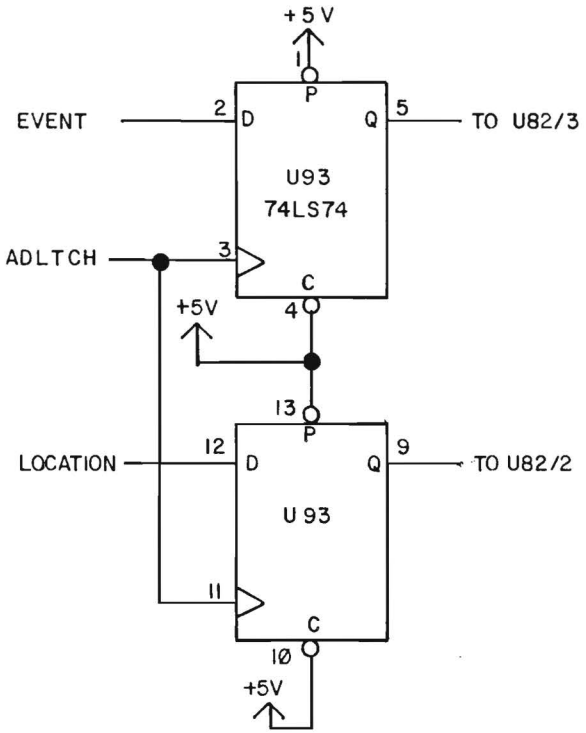
4.4 Write Sequence Controller

If the DX Interface is to extract adjacent or consecutive triggers, the speed of the Write Sequence Controller must be increased by at least a factor of 4. One way to gain significant performance improvement is to expand to a 32 bit format. In an "event", one 32 bit word could contain the -1 marker and address, while a second could contain the 32 bit clock. The maximum cycle time for the Write Sequence Controller is 600 ns.

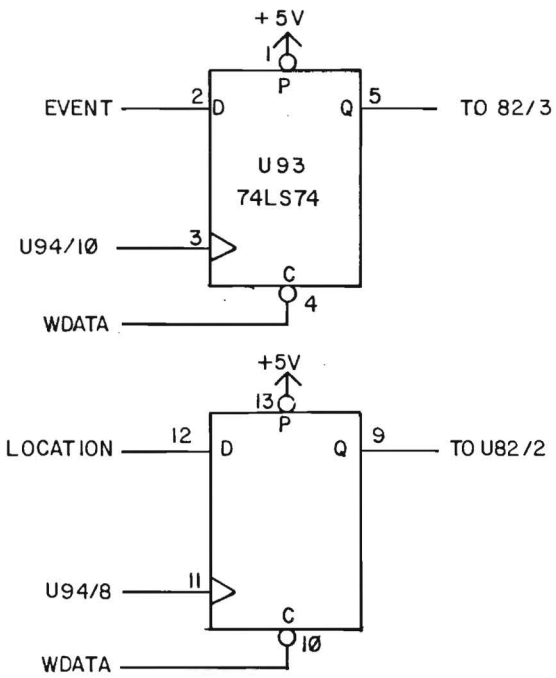
The current DX Interface requires that the two bit maps (location and event) be mutually exclusive. This limitation (from a hardware standpoint only) is due to the way U93 is connected to the rest of the circuit. Figure 6 shows a configuration of U93 which would allow an address to be a location or an event and thus increases the versatility of the DX Interface.

4.5 FIFO Buffer and DR11-B

The speed of the DR11-B will never allow full versatility of the DX Interface. As pointed out in Section 3, the DR11-B needs to be more than 10 times faster to allow extraction of completely general data. A decision will therefore have to be made on how large to make the FIFO to guarantee a useful system.



PRESENT



PROPOSED

NO.	DESCRIPTION OF CHANGE	CH.	DATE

SCALE: N.T.S. DATE: 3/30/82

CONTRACT NO. BED 21/21

PROJECT NO. A3183-000

ENGINEERING EXPERIMENT STATION
OF THE
GEORGIA INSTITUTE OF TECHNOLOGY
ATLANTA, GEORGIA

SCHEMATIC DIAGRAM–
MOD TO WRITE SEQUENCE
CONTROLLER

DR. COLEE
ENGR. T.E.T.
CH.
APP.

DRAWING NO.
A3183-006-E2

K+E DE 7382 19-1253

4.6 Conclusion

The current DX Interface will not operate at all with the EEPROM CPU. Some limited usefulness could be achieved by designing a new Write Sequence Controller capable of running at less than 600 ns per event or location. For full usefulness however, a much larger FIFO and faster DMA process are required.

When a second (slave) CPU is added, the Data Extraction process is going to be complicated by the sheer volume of the potential data. Some careful consideration should be given to the nature of the data to be extracted so that a useful DX Interface can be designed within reasonable limits of cost, power consumption, and maintainability.

GEORGIA TECH COMMENTS ON CONTROL PANEL
INTERFACE DESIGN REQUIREMENTS

1. COMPTEK should consider adding RAM to the adapter card and implementing Hi/Lo MEM on both master and slave. While this is beyond the original scope of the contract, it would not seriously affect design time or effort and would enhance the capability of the system.

2. The 9445 has a stack pointer and a frame pointer. Some provision should be made to allow these pointers to be examined and loaded from the console.

3. It is Georgia Tech's understanding that COMPTEK prefers a separate board for the slave CPU interface circuitry.

4. When the CPU is connected to the adapter card, J27 and J26 must be removed on the CPU card. This will disable the Auto-Restart function on the CPU card.

5. The adapter must have control of the latch which stores information from the ADDAT bus. This information includes address, memory data, and accumulator examines. When a CONREQ is pending, the console should not place the console code or switch data on the ADDAT bus until this data is requested from the adapter. This will eliminate bus contention on the ADDAT bus.

6. On APL, a "phantom" ROM can be inserted into the memory space, or the monitor routine can be transferred into valid RAM for direct execution. The "phantom" ROM approach will allow more flexibility and would be easer to design.

7. The detailed design of the control panel must be completed before the detailed adapter design can be finalized.

8. Georgia Tech will need at least the preliminary detailed design of the control panel before the detailed adapter design can begin.

9. When the EEPROM CPU is being used, all interface signals between adapter and control panel must be connected by the interface cable; that is, no signals can be connected via the back plane connector. This requirement is due to the fact that the slave control panel will not connect to the back plane.

10. To reduce the effects of transmission noise, all input signals should be buffered with a Schmitt-Trigger gate (74LS14 or equivalent). Provisions should be made on the P.C. board for the addition of terminating load resistors, should they become necessary. All output drives should be capable of driving 40 ma or more (8T98 or equivalent).

COMPTEK
RESEARCH INC.

MINUTES OF MEETING:
ISS MODICATIONS PROGRAM
ORIENTATION REVIEW

19 March 1982

Comptek Report No. 62K026001

Subcontract No. BED21121

Approved by: [redacted]
T. E. Tibbitts
GT-EES Project Director

Approved by: [redacted]
S. E. Cooper
Comptek ISS Program
Manager

1.0 Introduction

The orientation review for the ISS Modifications Program was held at GT-EES, Atlanta, Georgia on 11 and 12 March 1982. Attendees at the meeting were:

Steve Cooper	Comptek
Don Liedke	Comptek
Larry Holland	GT-EES
Dave Plummer	GT-EES
Terry Tibbitts	GT-EES
Henry Owen	GT-EES
Ken Trussell	GT-EES
John Parish	GT-EES

The Orientation Review was conducted for the following primary reasons:

a. To establish Comptek/GT-EES communications.
b. To mutually define the statement of work and its associated development schedule.
c. To define design requirements and technical risk areas.

The morning of 11 March was devoted to Comptek's presentation of the ISS Modifications Program requirements. Prior to the presentation, Comptek provided, for review and comment, copies of the "ISS Control Panel/Octal Display Interface Design Requirements" document. The presentation covered the following topics.

a. Orientation Review Objectives
b. ISS Development History and Future Development Plans
c. ISS System Description
d. ISS Operational Description
e. ISS Modifications Program Description
f. Program Organization
g. Comptek/GT-EES Liaison Requirements
h. Program Development Schedule
i. Technical Requirements

The afternoon of 11 March was devoted to GT-EES's technical presentation describing their approach to satisfying the Statement of Work (dated 26 February 1982) requirements developed by Comptek. The presentation covered the following topics.

a. Project Organization
b. Statement of Work Requirements
c. Deliverables
d. Technical Risks
e. Project Schedule
f. PDR Requirements

On the morning of 12 March, Mr. J. Lansford presented a technical description of the AN/ALR-46/69 EEPROM Upgrade and described GT-EES's current effort supporting the pre-production effort. Updated design data reflecting all technical changes to the CPU board were provided to Comptek by Mr. Tibbitts. The presentation and related discussions clarified several technical questions relating to dual-CPU operating protocol and requirements.

1.1 Scope

During the course of these presentations, the important points described in paragraph 1.2 were made. Paragraph 1.3 details the action items resulting from the review. Paragraph 1.4 specifies the changes to the Statement of Work (dated 26 February 1982) agreed upon. Paragraph 1.5 summarizes the changes of scope to the original Statement of Work which should be considered by GT-EES in preparing an updated formal price proposal.

1.2 Points of Discussion

The following points of discussion were made and resolved as described.

a. GT-EES recommended consideration of MIL-SPEC requirements in layout of EEPROM CPU boards.

b. GT-EES proposal reflects fabrication of two wire-wrap adapter cards (or one if both CPU adapter functions can be accommodated).

c. Informal monthly reports will be provided ten days after report period and include dollar and man-month estimates. Formal monthly report will be identical with respect to technical content.

d. Comptek will provide direction as to whether both CPU adapter functions should be incorporated on one board.

e. Comptek requires comments on CP Interface Design Requirements document prior to 26 March 1982.

f. Debug of the DR11-C parallel load function will be achieved during the integration period at Comptek, Buffalo.

g. Comptek will verify that ALR-46 group can make a modified EEPROM RWR available during WRALC integration.

h. Comptek will investigate the desirability of including RAM on one or both adapter cards such that EEPROM need not be disturbed in the RWR. Comment was made that this is currently out of scope.

i. This effort does not require demonstration of interprocessor communications or software structures to support this function. The requirement is to demonstrate only simultaneous processor control of and extraction from each CPU adapter function.

j. Design reviews at WRALC will require a technical status presentation by GT-EES which will be integrated within the overall Comptek presentation. GT-EES will not present separate schedule or cost information to WRALC.

k. The Comptek/GT-EES PDR and CDR reviews will occur during the same week as corresponding WRALC reviews. Comptek requires rough draft presentation material in Buffalo the Friday of the preceding week.

1. Based on prototype design, GT-EES requires approximately two weeks to fabricate a wire-wrapped CPU adapter card.

1.3 Action Items

The following action items were agreed upon:

Comptek:

a. Provide direction concerning adapter function implementation for 2 CPU's on one board prior to 26 March 1982.

b. Provide meeting minutes in the mail to GT-EES by 19 March 1982.

c. Provide decision as to whether RAM will be installed within the MASTER adapter function.

d. Provide outline for GT-EES final report which will satisfy Comptek's need to provide a Technical Manual for the interface adapter function.

GT-EES:

a. Provide proposal to be received in Buffalo on 19 March 1982 reflecting the considerations shown in the attachment. Attachment contents will be included in the meeting minutes. Proposal will be accompanied by staffing/task allocation profile by month.

b. Under current letter contract, proceed full speed with DX interface analysis and functional design of the CPU adapter.

c. Provide comments regarding Control Panel/Display Design Requirements by 26 March 1982.

1.4 Changes to Statement of Work

The following changes to the Statement of Work, dated 26 February 1982, were agreed upon:

a. Paragraph 2.2a - Change "four weeks" to "six weeks".

b. Paragraph 2.4.1, second bullet item - Add sentence; "Red-lined updates to the preliminary designs are desired".

c. Paragraph 4.0(d) - Change "7 months" to "6 1/2 months".

d. Paragraph 4.0(d), second bullet item - Change "(4 weeks)" to "(6 weeks)".

e. Paragraph 4.0(f), bullet item - Change "updates" to "red-lined updates".

f. Paragraph 5.0, next to last sentence - Change "14" to "12".

1.5 GT-EES Proposal Considerations

In preparing an updated formal price proposal to Comptek, GT-EES will consider the following points.

a. Ensure the proposal reflects reduction of effort and materials in the following areas:

   1. Elimination of DX design, implementation, and testing requirements.

   2. Elimination of production phase costs with the exception of on-call engineering support to Comptek subsequent to the final design package delivery. One-man month should be sufficient.

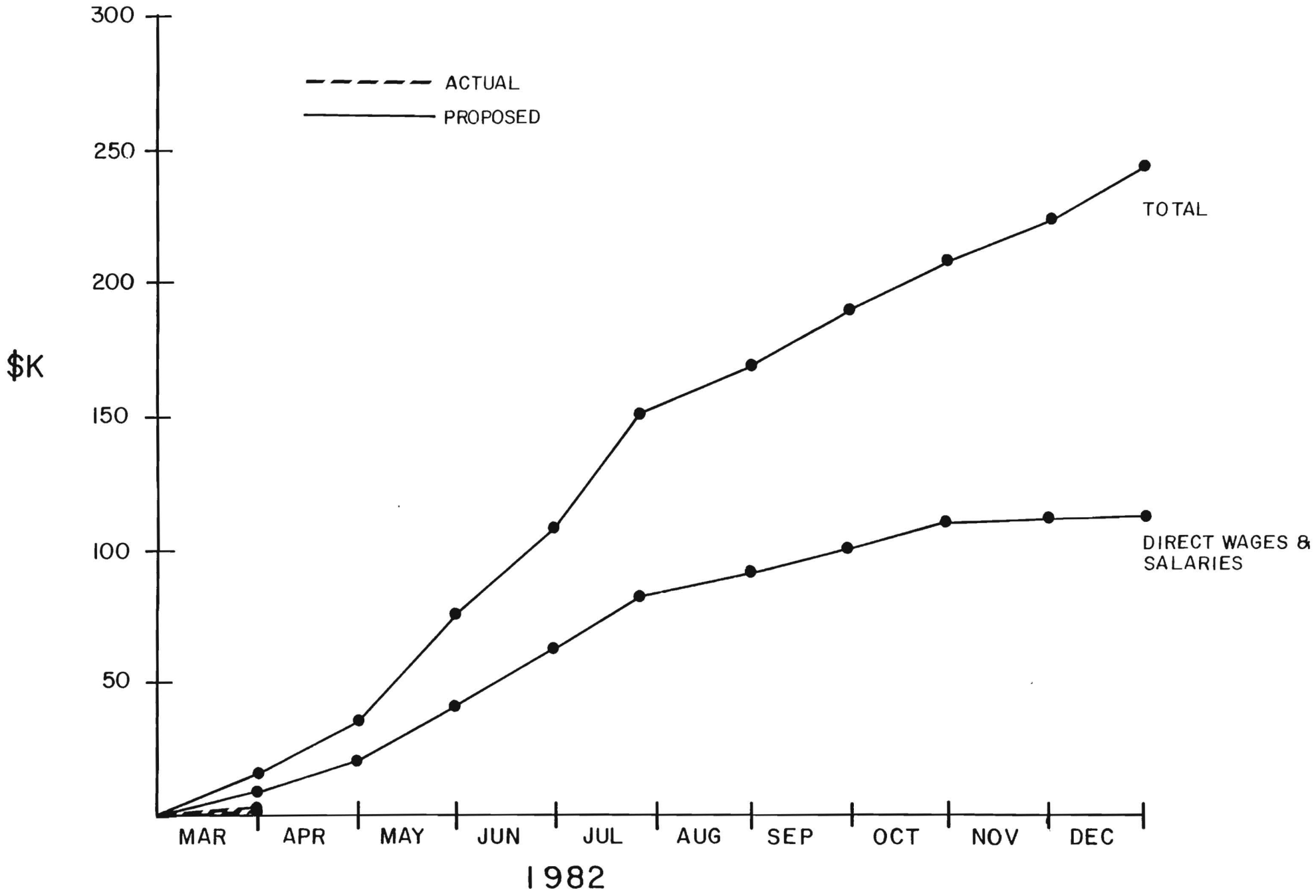
   3. Elimination of user manual input requirement.

4. Elimination of formal design data update (SOW item 4.0(e)).

b. Ensure the proposal reflects increase in effort to support item 2.1.1 in the SOW (microcomputer CCA support).

c. Proposal should reflect a performance period of 12 months vs. 14 months shown in presentation.

A3183 PROJECTED/ACTUAL EXPENDITURES



Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

20 May 1982

COMPTEK Research, Incorporated
One Technology Center
45 Oak Street
Buffalo, New York 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject subcontract for the period 1 April 1982 to 30 April 1982 is presented herein.

The intent of this program is to design, build, and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During the month of April, the basic design (block diagram/signal flow level) was completed. This basic design will be the starting point for the detailed design which will begin upon approval of the basic design by COMPTEK.

Preparations for the Preliminary Design Review (scheduled for the first of May) were started.

The question of RAM on the adapter card has been settled with all sides agreeing that it is not desirable to have RAM on the adapter card.

Problem Areas

Both COMPTEK and Georgia Tech EES need to get together to discuss options on placing the DX circuitry on the adapter card. However, this is not currently a pressing item and will probably not become critical until fabrication is started on the adapter card.

No major technical problems are known at this time.

Summary of Project Meetings

No project meetings were held during April.

Summary of Cost Incurred

The following costs were incurred:

	Month	Total
Direct Salaries	$4,807.04	$6,239.09
Retirement	517.57	679.03
Travel	-0-	-0-
Materials & Supplies	228.11	239.93
Overhead (55%)	3,054.00	3,936.93
TOTAL	$8,606.72	$11,094.98

Expected Technical Activities

The Preliminary Design Review is currently scheduled for the first of May. Based on approval of the Preliminary Basic Design at that time, Georgia Tech will begin the detailed design immediately. Discussions on DX options should continue.

Respectfully submitted,

[redacted]

Terry Tibbitts
Project Director

TET/dta

APPROVED:

[redacted]

David K. Plummer, Head
Surveillance Technology Branch

A-383

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

11 June 1982

COMPTEK Research, Incorporated
One Technology Center
45 Oak Street
Buffalo, New York 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract Number BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject subcontract for the period 1 May 1982 to 31 May 1982 is presented herein.

The intent of this program is to design, build, and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During the month of May, the detailed design of the EEPROM CPU adapter was started. A preliminary set of schematics should be completed early in June and will be sent to COMPTEK immediately upon completion for review.

Some questions have arisen about the Display/Control Panel design. These are:

1. A separate STOP switch is not desired on a 9445 design. The 9445 has a console code for STOP but no separate input line capable of halting the 9445.

2. If LOW MEM/HI MEM are not going to be implemented (indicated as a possibility during the PDR), then it would simplify the adapter design to encode EXA SP with LHH instead of LLL. Even if LOW MEM/HI MEM are used, this code could be shared with LOW MEM because LOW MEM is not used in the EEPROM configuration and SP is not used in the non-EEPROM configuration.

   Long lead-time parts are now being ordered to insure a smooth prototype construction phase.

Problem Areas

No technical problems are known at this time.

Summary of Project Meetings

The Preliminary Design Review was held the first week of May. At that time options were discussed on the physical location of the DX circuitry. It was decided to pursue a single board design with the DX and adapter circuitry on a single card. The details of this approach are yet to be worked out.

Summary of Cost Incurred

The cost estimate has been revised downward to $190,000. A new plot of projected expenditures is attached with actual expenditures to date.

The following costs were incurred:

	Month	Total
Direct Salaries	$ 5,865	$12,104
Retirement	581	1,260
Travel	40	40
Materials and Supplies	974	1,214
Overhead (55%)	4,103	8,040
TOTAL	$11,563	$22,658

Expected Technical Activities

The detailed design should be completed in early June. Fabrication will begin upon approval of the detailed design by COMPTEK.

Respectively submitted,

[redacted]

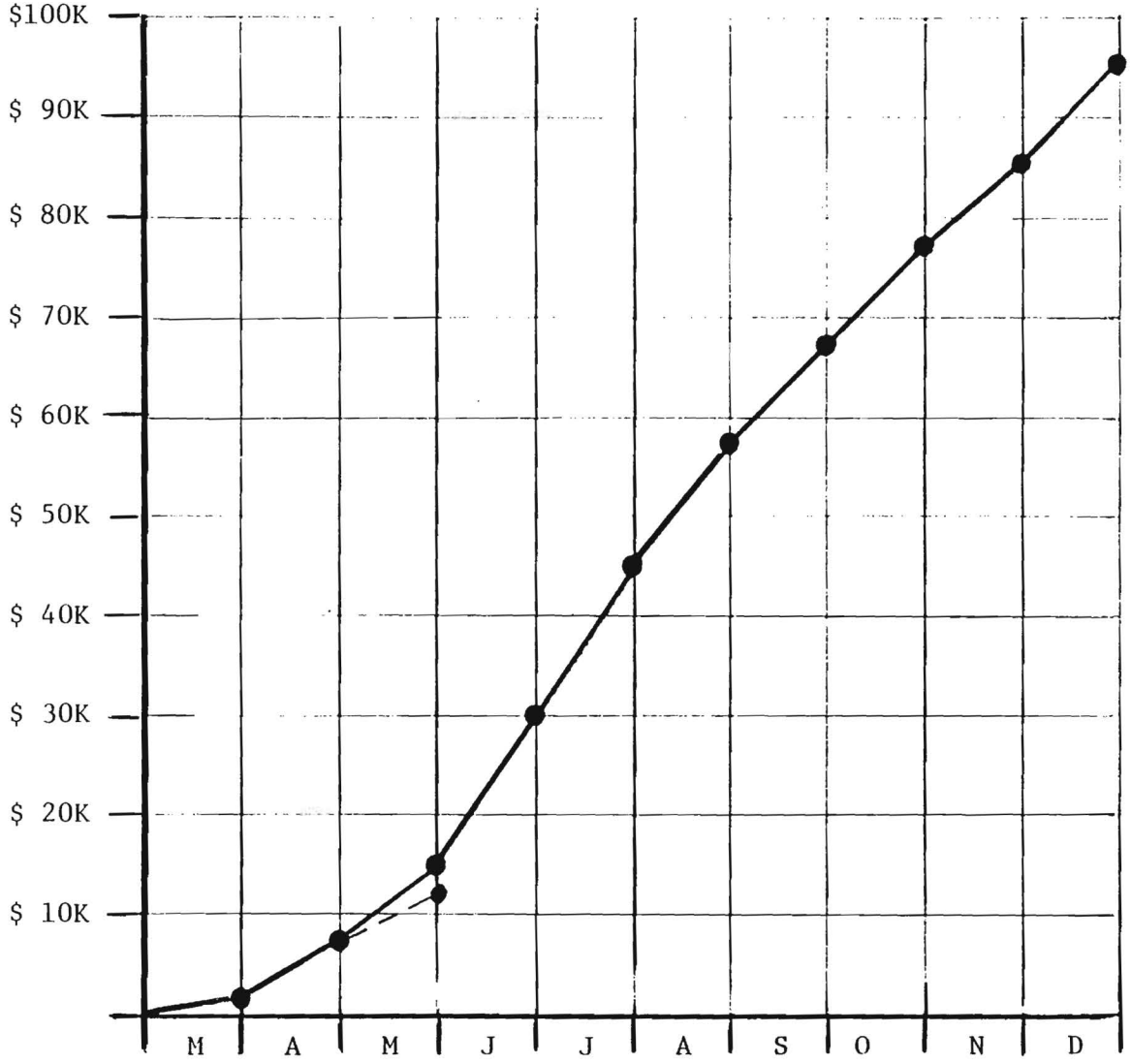
Terry E. Tibbitts
Project Direct

TET/dta
Attachment

APPROVED:

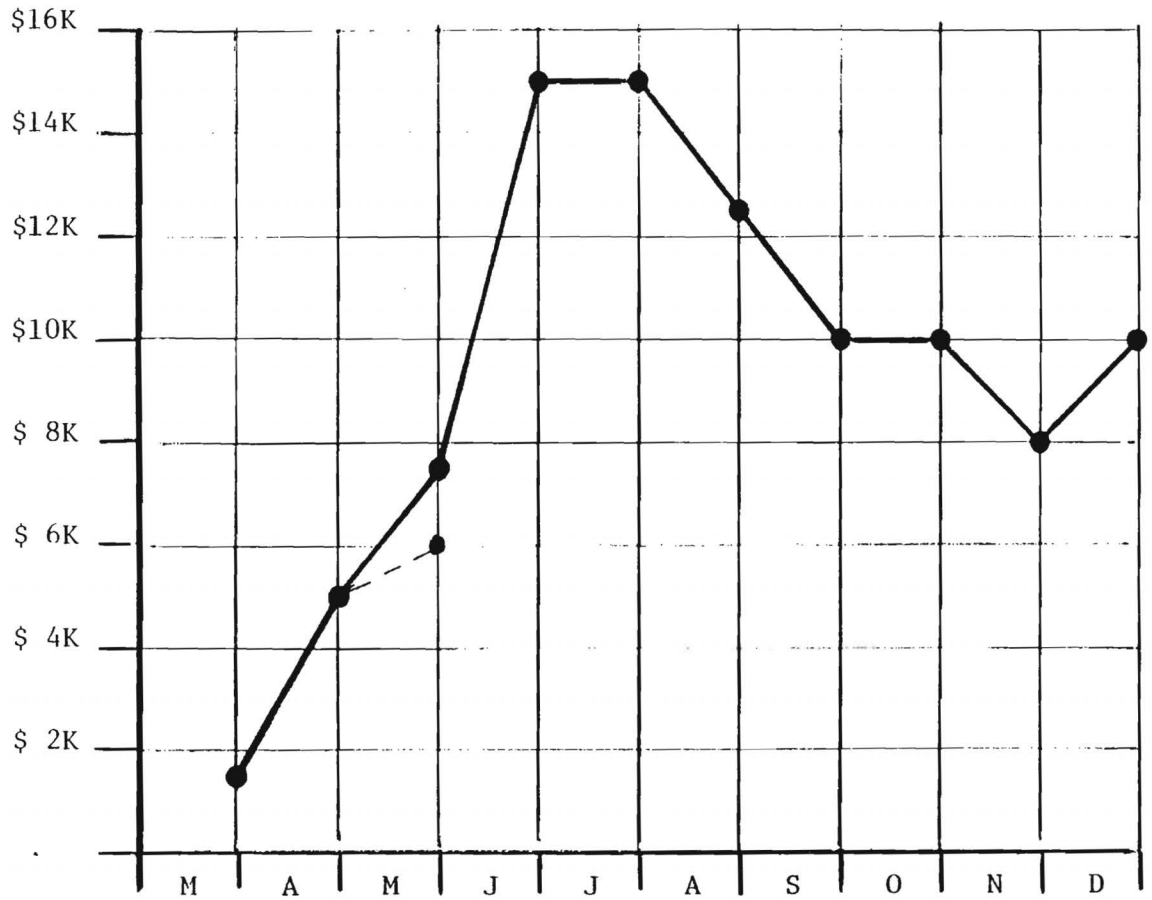
[redacted]

D. K. Plummer, Head
Surveillance Technology Branch



PROJECTED ACCUMULATED EXPENDITURES

(Direct Salaries & Wages)



PROJECTED MONTHLY EXPENDITURES

(Direct Salaries & Wages)

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

30 June 1982

COMPTEK Research, Incorporated
One Technology Center
45 Oak Street
Buffalo, New York 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract Number BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject subcontract for the period 1 June 1982 to 30 June 1982 is presented herein.

The intent of this program is to design, build, and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During the month of June, the detailed design of the EEPROM CPU adapter was completed. Approval was given by COMPTEK for Georgia Tech to begin construction of the wire-wrap prototype. This prototype will be completed early in July.

During the 10 June design meeting, COMPTEK requested a list of the new device codes added to the RWR system. This list is attached. Currently the I/O bus buffer assumes all input devices (devices which are read by the CPU) between 1Ø and 27 octal reside outside the processor box. Individual device codes outside this range can be added as needed by reprogramming the PAL which controls the bus buffer direction. All output devices (devices written to by the CPU) can be on either side of the bus buffer.

It has been determined that the only cable modification to the ISS required by the EEPROM adapter will be the addition of the 50-pin ribbon cable connecting the EEPROM CPU to the adapter and the 40-pin ribbon cable connecting the adapter to the control panel.

CPU Modifications

It has been learned that the older ALR-46 power supplies have a very long turn on time which was causing a problem with the power up reset. To solve this problem, C1 was changed from 4.7 µF to 39 µf and R3 was changed from a 10K resistor to a 1N4002 diode.

A change in the EEPROM specification requires the reprogramming voltage to be changed from 21V to 21.5V. This is accomplished by changing R18 from 30.22K ± 0.5% to 44.6K ± 0.5% and R19 from 62.69K ± 0.5% to 95.1K ± 0.5%

Problem Areas

The 10 MHz signal connects into the old adapters via J101-55. This connector is being eliminated on the new adapters; therefore, if 10 MHz is required in the NOVA chassis, a cable modification or an oscillator on the adapter card will be necessary.

No other problems are known at this time.

Summary of Project Meetings

On 10 June 1982, John Parish and Terry Tibbitts visited COMPTEK to discuss the detailed adapter design. The Georgia Tech action items were:

1. Incorporate all changes discussed and provide updated logics to COMPTEK.

2. Provide list of new device codes.

Summary of Costs Incurred

The following costs have been incurred:

	MONTH	TOTAL
Direct Salaries	$ 9,419	$21,523
Retirement	942	2,202
Travel	1,057	1,097
Materials and Supplies:	264	1,478
Overhead (55%):	6,425	14,465
TOTAL	$18,107	$40,765

Expected Technical Activities

During July, fabrication of the prototype adapter will be completed. A subset of the control panel logic will be implemented to aid in testing the adapter.

Respectfully submitted,

[redacted]

Terry E. Tibbitts
Project Director

TET/dta
Attachment

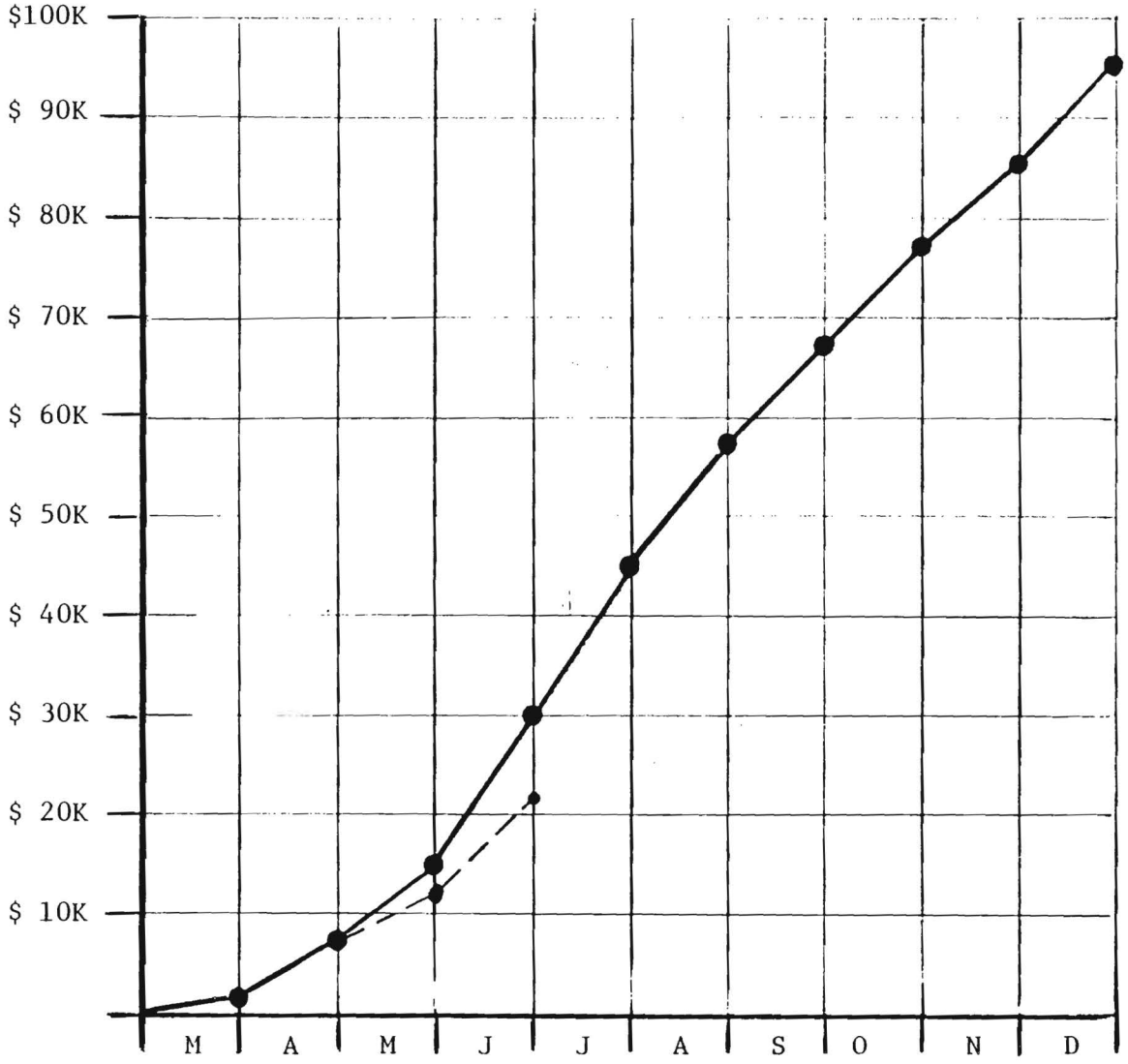
APPROVED:

[redacted]

D. K. Plummer, Head
Surveillance Technology Branch

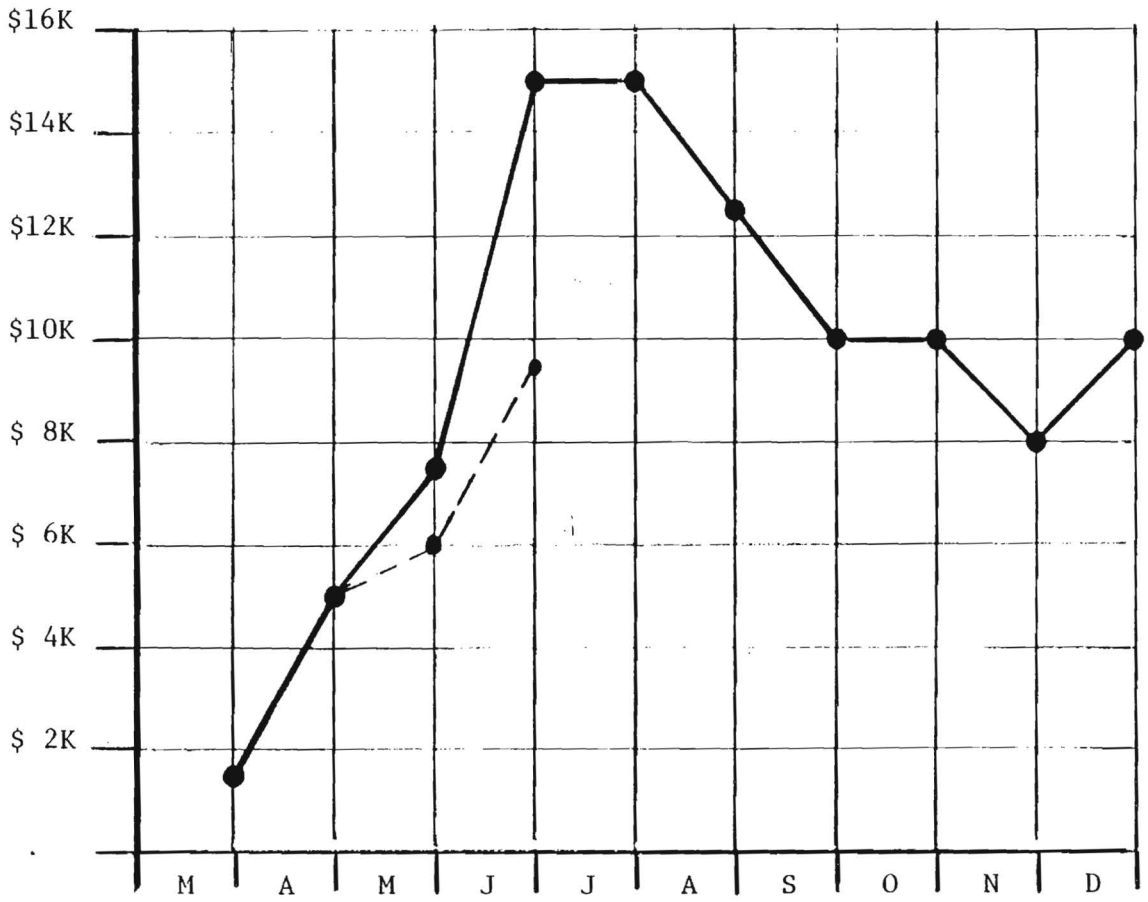
NEW DEVICE CODES

NIOS 64	Turn on 25 volts for EEPROM programming. This must be followed by a 'STA' instruction to reprogram EEPROM.
NIOC 66	Clear the counter which counts the return pulses from the RWR processor.
NIOS 67	Start the serial output from the output registers to the RWR.
DIA AC, 66	Read the pulse counter giving the current number of pulses returned.
DOA AC, 67	Load the 16-bit output register with the first 16-bits of the 22 bit word being sent.
DOB AC, 67	Load the 6-bit output register with the last 6 bits of the 22-bit word being sent. Note: These should be in the most significant position of the AC and bit 5 is the first bit to be sent of the 22 bits (i.e., least significant bit first).
DIA AC, 70	Read the L/V front panel mode switch. Bit 15 = 1 if in 'Load Tape' position Bit 15 = 0 if in 'Transmit' position
DOA AC, 70	Write an ASCII character to a display Bit 0-7 = index into display (0-23) Bit 8-15 = ASCII character to display
NIOC 70	Blank the display.
NIOS 70	Unblank the display.
SKPBN 70	Continue switch. Pressed when busy is non-zero.
DOA 65	Write to DMA register.
DIA 65	Read DMA register.
DOB 65	Write Slave Port.
DIB 65	Read Slave Port.



PROJECTED ACCUMULATED EXPENDITURES

(Direct Salaries & Wages)



PROJECTED MONTHLY EXPENDITURES

(Direct Salaries & Wages)

A-3783

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

9 August 1982

Comptek Research, Inc.
One Technology Center
45 Oak Street
Buffalo, NY 14203

ATTENTION: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract Number BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject subcontract for the period 1 July 1982 to 21 July 1982 is presented herein.

The intent of this program is to design, build, and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During the month of July, the CPU adapter and a subset of the control panel logic were fabricated. At the 20-21 July Critical Design Review, these two boards were presented and discussed. All changes agreed upon by Georgia Tech, Comptek, and WRALC have been incorporated into the board. The changes included:

1. Addition of Master/Slave arbitration hardware.
2. Three-state control of all DX signals.
3. Addition of a 50 pin ribbon connector containing all DX signals.
4. Correcting minor logic problems.

The control panel logic was also updated to reflect current Comptek documentation.

Attached is a pin connection list for the temporary DX connector. This connector is being provided to allow for independent construction of the DX and adapter functions.

Currently, the logic equations for the Programmable Array Logic (PAL) are being entered into a Nova Computer. Hardware testing will begin as soon as these equations are debugged (first two weeks in August).

Problem Areas

No problems are known at this time.

Summary of Project Meetings

The critical design review was held on 20-21 July. The Georgia Tech action items were:

1. Incorporate all logic changes on adapter and control panel.
2. Provide pin list for DX connector.
3. Proceed with testing.
4. Aid in the debug of the Comptek CPU card when it becomes available.
5. Design Master/Slave arbitration hardware.

Summary of Cost Incurred

Direct Salaries	$ 7,947	$29,470
Fringe	1,350	3,552
Travel	63	1,160
Materials and Supplies	885	2,363
Overhead	4,835	19,300
TOTAL	$15,080	$55,845

Expected Technical Activities

During August, testing will begin on the adapter hardware. Testing should be completed by late August or early September with shipment of hardware (to Comptek) following immediately.

Respectfully submitted,

[redacted]

Terry E. Tibbitts
Project Director

Approved:

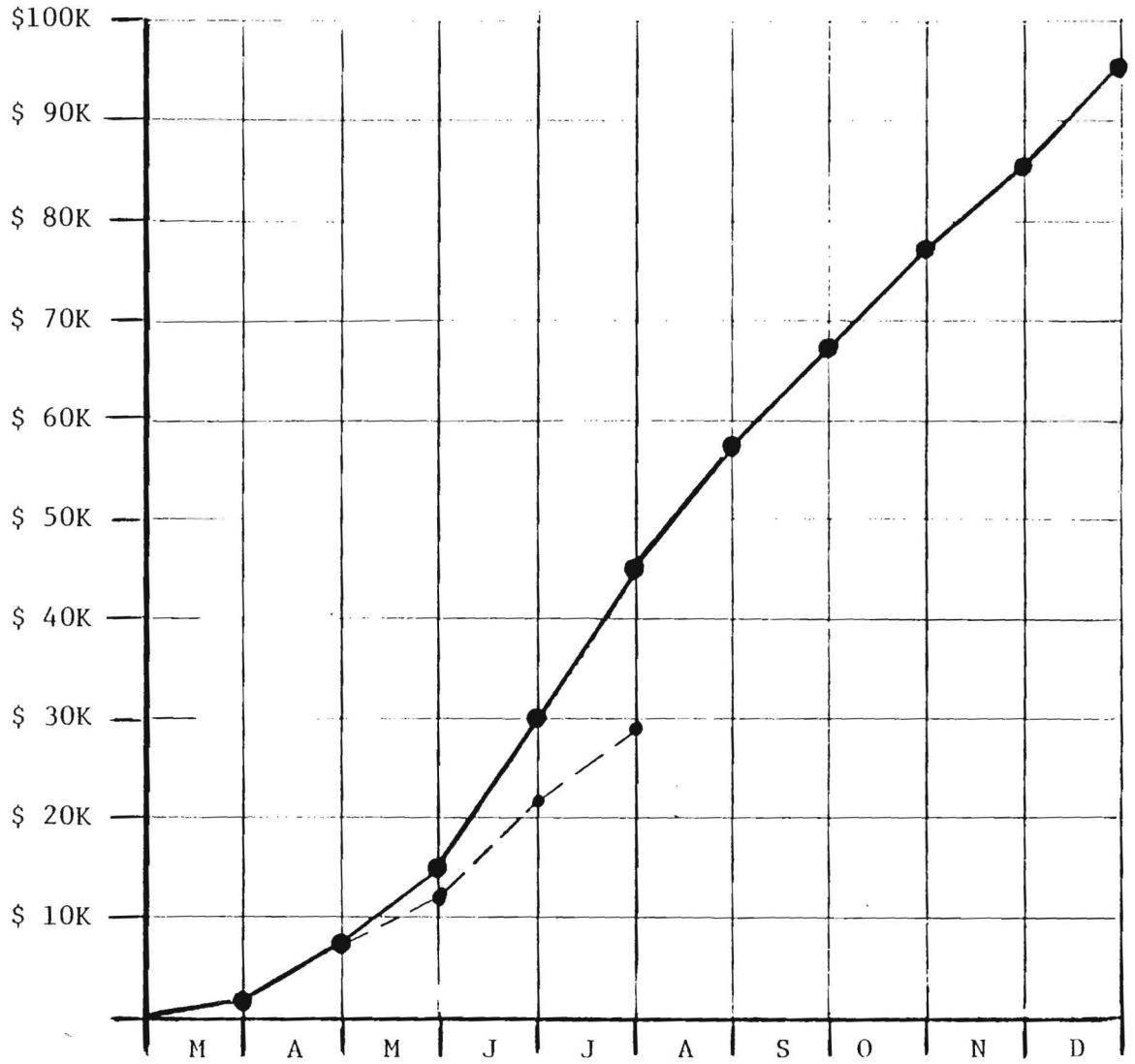
[redacted]

David K. Plummer, Head
Surveillance Technology Branch

TET/djs

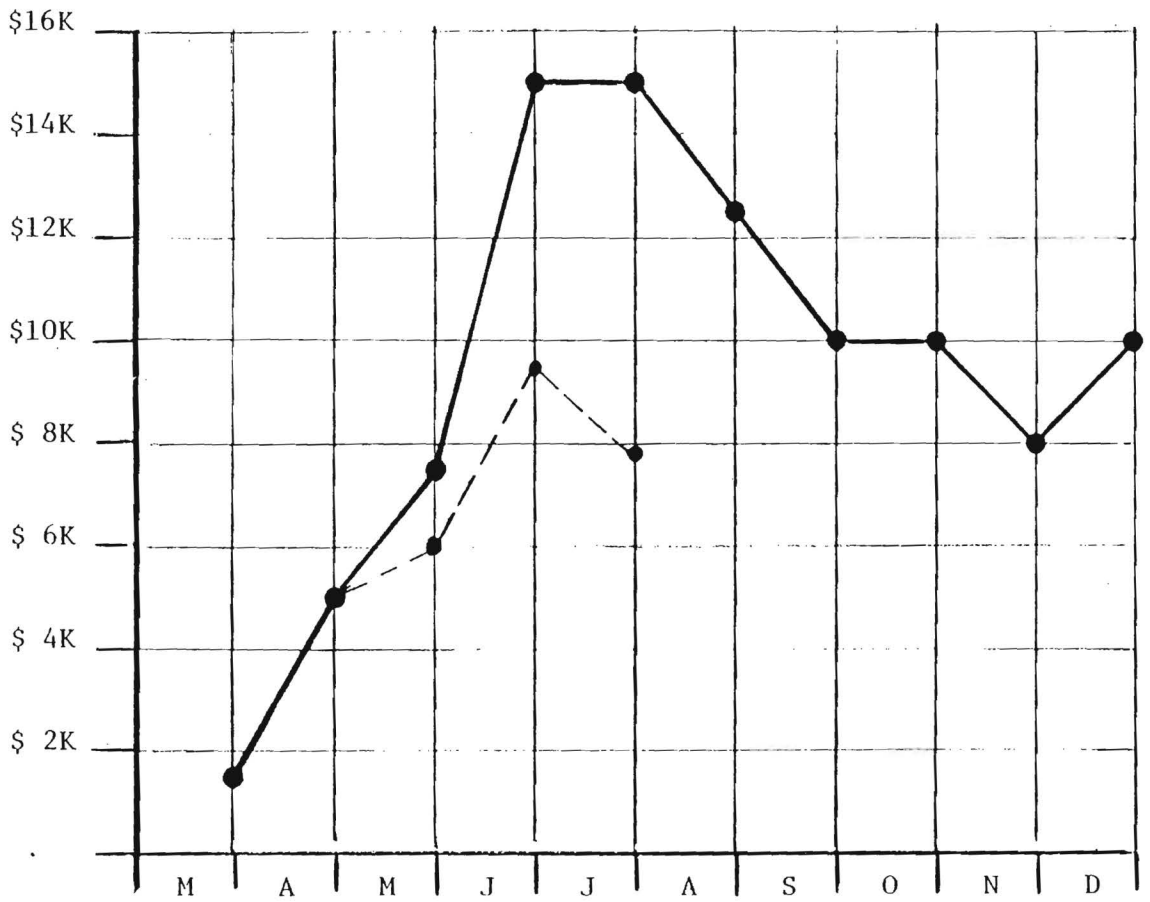
DX Connector

J3-1	DATA Ø	J3-2	ADD Ø
J3-3	DATA 1	J3-4	ADD 1
J3-5	DATA 2	J3-6	ADD 2
J3-7	DATA 3	J3-8	ADD 3
J3-9	DATA 4	J3-10	ADD 4
J3-11	DATA 5	J3-12	ADD 5
J3-13	DATA 6	J3-14	ADD 6
J3-15	DATA 7	J3-16	ADD 7
J3-17	DATA 8	J3-18	ADD 8
J3-19	DATA 9	J3-20	ADD 9
J3-21	DATA 10	J3-22	ADD 10
J3-23	DATA 11	J3-24	ADD 11
J3-25	DATA 12	J3-26	ADD 12
J3-27	DATA 13	J3-28	ADD 13
J3-29	DATA 14	J3-30	ADD 14
J3-31	DATA 15	J3-32	ADD 15
J3-33		J3-34	FETCH -
J3-35	BSTOPPED	J3-36	DXR -
J3-37	RESET -	J3-38	DXW -
J3-39		J3-40	
J3-41		J3-42	
J3-43		J3-44	
J3-45		J3-46	
J3-47		J3-48	
J3-49		J3-50	



PROJECTED ACCUMULATED EXPENDITURES

(Direct Salaries & Wages)



PROJECTED MONTHLY EXPENDITURES

(Direct Salaries & Wages)

A-3109

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

21 September 1982

Comptek Research, Inc.
One Technology Center
45 Oak Street
Buffalo, N.Y. 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject subcontract for the period 1 August 1982 to 31 August 1982 is presented herein.

The intent of this program is to design, build and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During the month of August, all testing which could be done at Georgia Tech was completed. Final testing will require a fully operational front panel available only at Comptek.

All problems that were encountered during testing have been corrected. These problems were minor, consisting mostly of wiring errors.

Problem Areas

No problems are known at this time.

Summary of Project Meeting

No project meetings were held in August.

Summary of Cost Incurred

	August	Total
Direct Salaries	$ 8,016	$37,486
Fringe	1,389	4,941
Travel	214	2,576
Materials and Supplies	6	1,166
Overhead	4,535	23,835
TOTAL	$14,160	$70,004

Expected Technical Activities

A one-week trip is planned early in September to Comptek for the completion of testing and delivery of the first prototype EEPROM CPU adapter. At the end of this testing period, a second adapter will be fabricated to test master/slave operation.

Respectfully submitted,

[redacted]

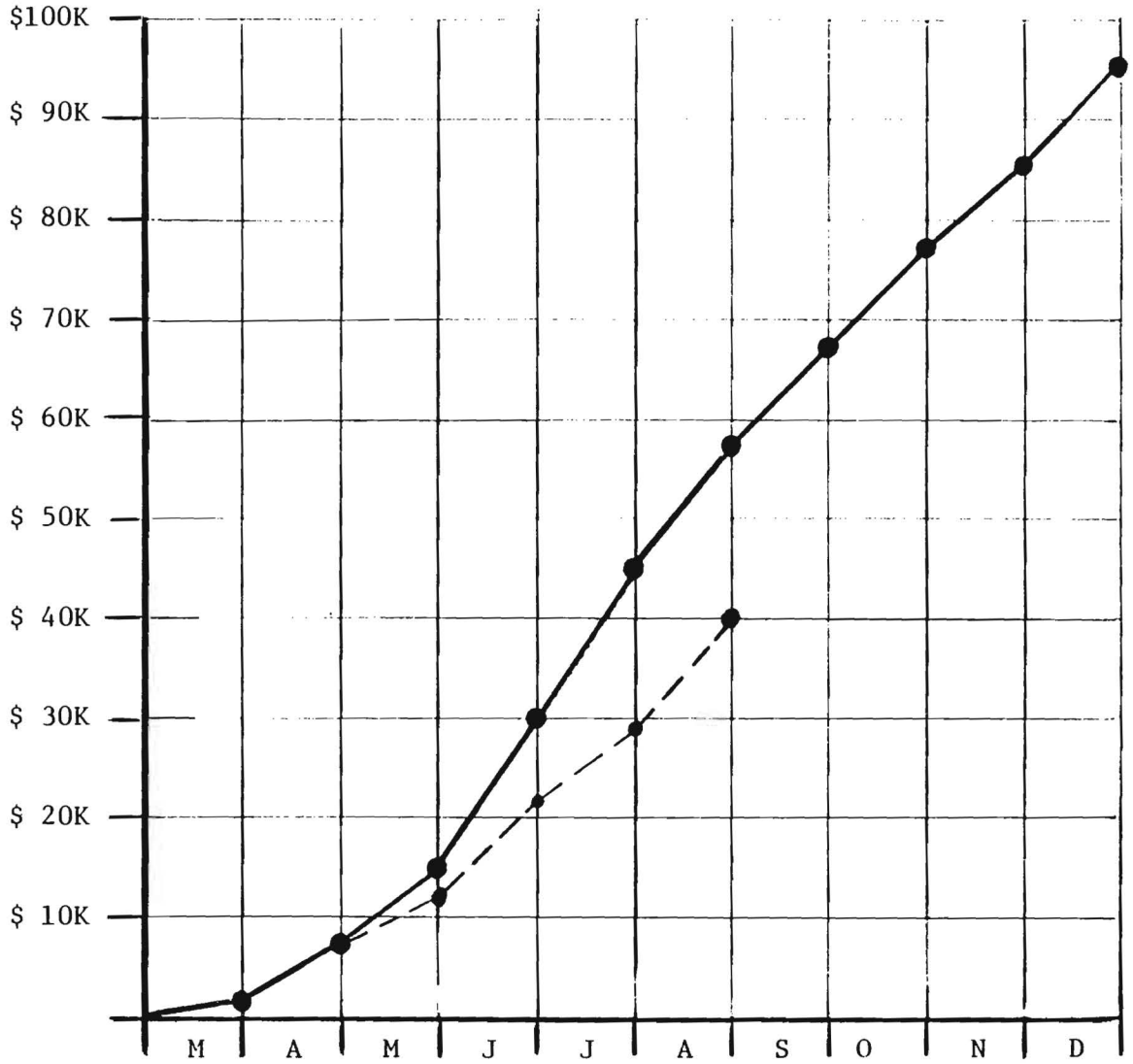
Terry E. Tibbitts
Project Director

Approved:

[redacted]

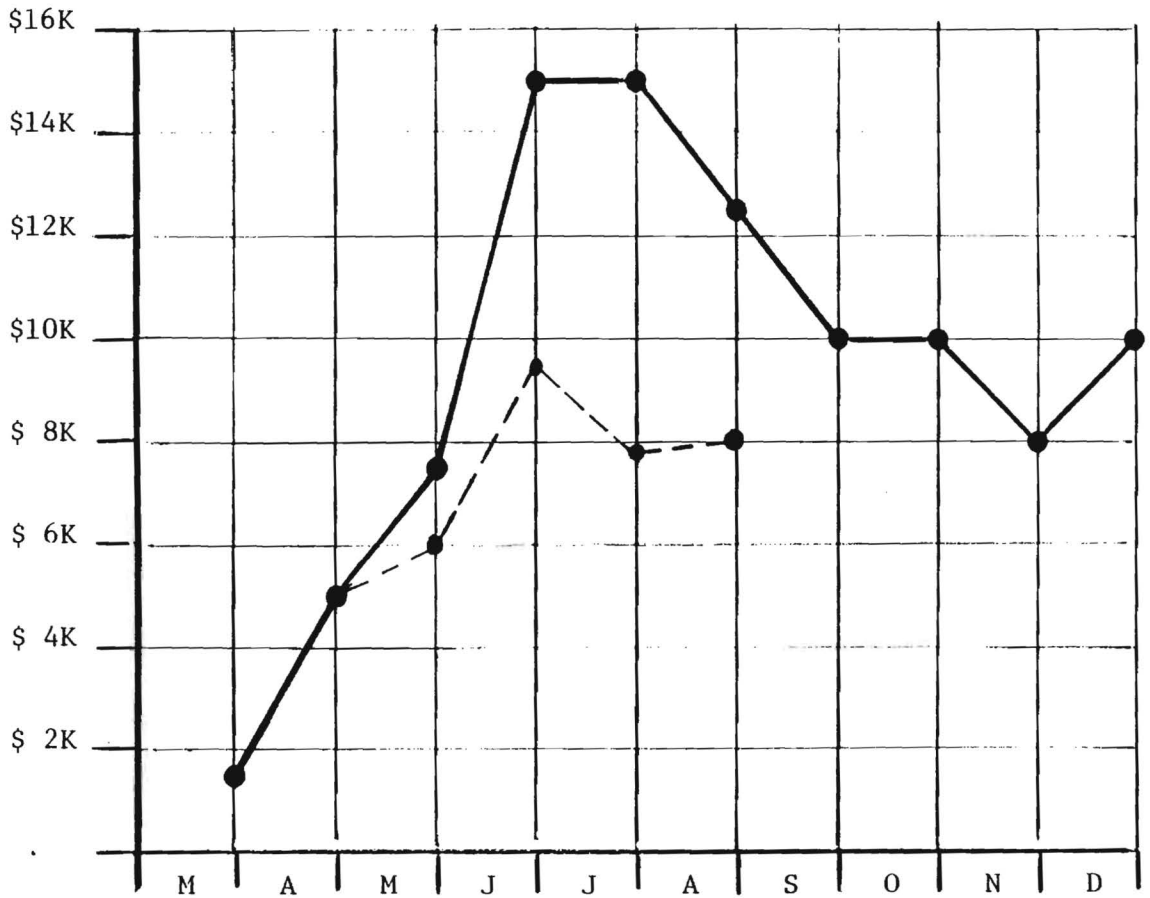
David K. Plummer, Head
Surveillance Technology Branch

TET/djs



PROJECTED ACCUMULATED EXPENDITURES

(Direct Salaries & Wages)



PROJECTED MONTHLY EXPENDITURES

(Direct Salaries & Wages)

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

18 October 1982

Comptek Research, Inc.
One Technology Center
45 Oak Street
Buffalo, NY 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject sub-contract for the period 1 September 1982 to 30 September 1982 is presented herein.

The intent of this program is to design, build and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During September, the first EEPROM adapter was delivered to Comptek during a one week trip by John Parish and Terry Tibbitts. For the first time, all components of the adapter/front panel system were connected and tested together.

No major problems were encountered during this test phase and Comptek instructed Georgia Tech to continue with fabrication of the second adapter board. This board will be used to test master/slave operations. A second trip to Comptek is currently planned for the week of 11 October 1982 to deliver this board. As per agreement between Comptek and Georgia Tech, the second board will not contain the DX circuitry, but will have a 50 pin connector for interfacing the DX card and adapter card.

Problem Areas

A problem was discovered in the instruction step circuitry. If a software HALT is encountered while stepping through memory, the CPU will repeat the HALT instruction indefinitely. This is due to the internal operation of the Program Counter and the Exam Memory in the examine sequence of the front panel circuitry. A solution is being investigated and it is felt the problem can be easily solved.

The FETCH signal being supplied to the DX interface logic was found to be undesirable because the address was not stable at the start of the FETCH signal. A new signal called DXFETCH has been added to solve this timing problem.

Summary of Project Meeting

No project meetings were held in September.

Summary of Cost Incurred

	Sept.	Total
Direct Salaries	$ 9,354	$46,842
Fringe	1,360	6,301
Travel	752	1,917
Materials and Supplies	409	2,985
Overhead	5,605	29,440
TOTAL	$17,480	$87,485

Expected Technical Activities

A one week trip is scheduled for 11 October 1982 to deliver the second adapter board. This board will be used to test master/slave operations.

Respectfully submitted,

[redacted]

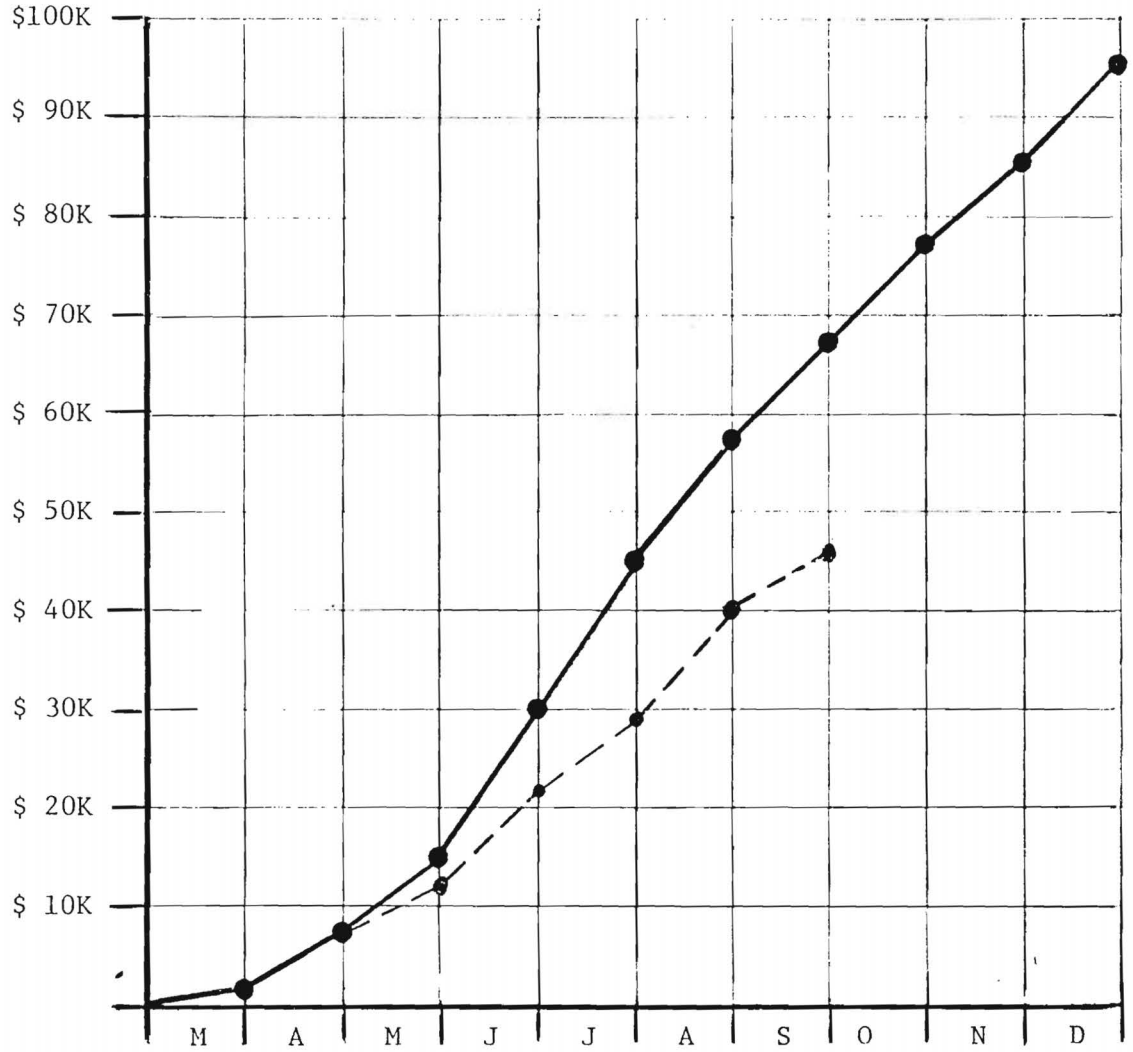
Terry E. Tibbitts
Project Director

Approved:

[redacted]

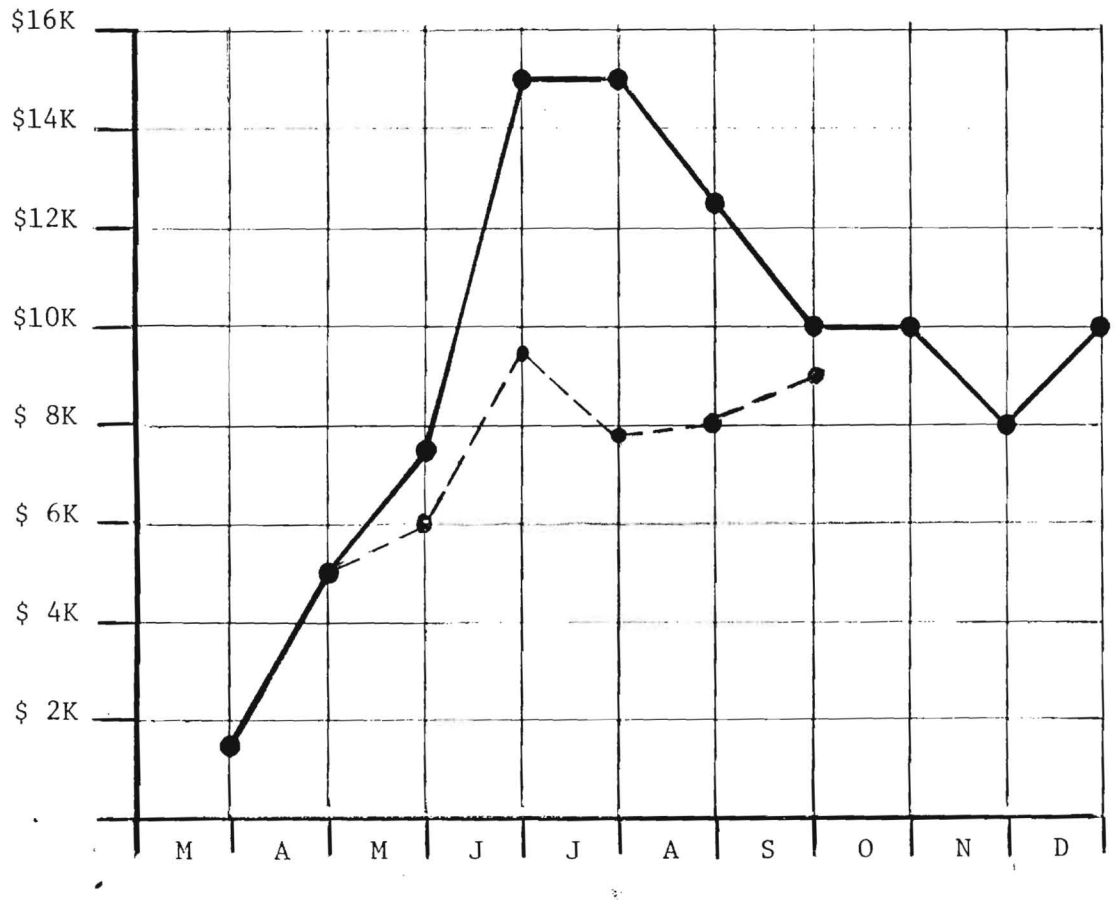
D. K. Plummer, Head
Surveillance Technology Branch

TET/djs



PROJECTED ACCUMULATED EXPENDITURES

(Direct Salaries & Wages)



PROJECTED MONTHLY EXPENDITURES

(Direct Salaries & Wages)

A-3188

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

15 November 1982

Comptek Research, Inc.
One Technology Center
45 Oak Street
Buffalo, NY 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject sub-contract for the period 1 October 1982 to 30 October 1982 is presented herein.

The intent of this program is to design, build and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

During October, the second adapter board was completed and delivered to Comptek Research, Inc. After three (3) days of integration testing, all minor problems were corrected. Comptek later made a cable modification to reduce noise on the I/O lines inside the adapter chassis.

At this point, all hardware has been demonstrated successfully with dual CPU operation and all known technical problems associated with front panel operation have been solved.

Preliminary work on documentation associated with the final report has begun. Detailed work on the final report will be started upon receipt of a suggested format from Comptek.

Problem Areas

No problems are known at this time.

Summary of Project Meeting

No project meetings were held in October.

Expected Technical Activities

A one week trip is scheduled for 15-19 October 1982 to WRALC for prototype system delivery. Georgia Tech will have personnel at WRALC to aid in troubleshooting any last minute problems.

Summary of Cost Incurred

	Oct.	Total
Direct Salaries	$ 6,432	$53,273
Fringe	1,188	7,490
Travel	1,588	3,506
Materials and Supplies	270	3,254
Overhead	4,474	33,914
TOTAL	$13,952	$101,437

Respectfully submitted,

[redacted]

Terry E. Tibbitts
Project Director

Approved:

[redacted]

D. K. Plummer, Head
Surveillance Technology Branch

TET/djs

Georgia Institute of Technology
ENGINEERING EXPERIMENT STATION
ATLANTA, GEORGIA 30332

1 December 1982

Comptek Research, Inc.
One Technology Center
45 Oak Street
Buffalo, NY 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject sub-contract for the period 1 November 1982 to 30 November 1982 is presented herein.

The intent of this program is to design, build and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

All design and construction activity associated with this sub-contract was completed during November. The technical documentation is the only outstanding item. This technical documentation consists of finished schematics, theory of operation, and final report.

Summary of Costs Incurred

	Nov.	Total
Direct Salaries	$ 5,743	$ 59,016
Fringe	1,085	8,575
Travel	-0-	3,506
Materials and Supplies	210	3,464
Overhead	3,322	37,236
TOTAL	$10,360	$111,797

Estimated Cost of Technical Documentation

It is estimated that it will take two months (December and January) to complete the technical documentation.

Direct Salaries	$13,000
Fringe	2,000
Travel	-0-
Materials and Supplies	500
Overhead	7,500
TOTAL	$23,000

Respectfully submitted,

[redacted]

Terry E. Tibbitts
Project Director

Approved:

[redacted]

D. K. Plummer, Head
Surveillance Technology Branch
Systems Engineering Laboratory

TET/djs

ENGINEERING EXPERIMENT STATION
Georgia Institute of Technology
A Unit of the University System of Georgia
Atlanta, Georgia 30332

15 February 1983

Comptek Research, Inc.
One Technology Center
45 Oak Street
Buffalo, NY 14203

Attention: Mr. Tom Ciaccia
Mr. Steve Cooper

Reference: Sub-Contract No. BED 21121

Subject: Engineering Management Report

Gentlemen:

A summary of the progress on the subject sub-contract for the period 1 December 1982 to 31 January 1983 is presented herein.

The intent of this program is to design, build and test a prototype EEPROM CPU adapter for the Integrated Support Station (ISS).

Summary of Technical Activities

All design and construction activity associated with this sub-contract has been completed. The technical documentation is the only outstanding item. This technical documentation consists of finished schematics, theory of operation, and final report.

Summary of Costs Incurred

	Dec./Jan.	Total
Direct Salaries	$ 9,104	$ 68,120
Fringe	1,841	10,416
Travel	301	3,807
Materials and Supplies	178	3,642
Overhead	5,392	42,628
TOTAL	$16,816	$128,613

Estimated Cost of Completion

It is estimated that it will take the following to complete the technical documentation.

Direct Salaries	$ 4,000
Fringe	600
Travel	-0-
Materials and Supplies	300
Overhead	2,000
TOTAL	$ 6,900

Respectfully submitted,

[redacted]

Terry E. Tibbitts
Project Director

Approved:

[redacted]

D. K. Plummer, Head
Surveillance Technology Branch
Systems Engineering Laboratory

TET/djs

FINAL REPORT

GT/EES PROJECT NO. A-3183

EEPROM CPU ADAPTER DEVELOPMENTAL DESIGN DATA AND TECHNICAL MANUAL

Prepared for

COMPTEK RESEARCH, INC.
45 OAK STREET
BUFFALO, N.Y. 14203

Under

Sub-Contract No. BED 21121

March 1983

GEORGIA INSTITUTE OF TECHNOLOGY

A Unit of the University System of Georgia
Engineering Experiment Station
Atlanta, Georgia 30332

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"EEPROM/CPU ADAPTER DEVELOPMENTAL DESIGN DATA AND TECHNICAL MANUAL"

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T. E. Tibbitts
J. T. Parish

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GEORGIA INSTITUTE OF TECHNOLOGY
Engineering Experiment Station
Systems Engineering Laboratory
Electronic Support Measures Division
Atlanta, Georgia 30332

FOREWORD

This report presents details of a ground support equipment upgrade program whose primary objective was to develop a prototype adapter board capable of interfacing the newly developed EEPROM/Central Processing Unit (CPU) of the AN/ALR-46,-46A, and -69 Radar Warning Receivers with the computer control panel of the AN/ALR-46/69 Integration Support Stations (ISSs). The ISS is a ground based, fixed station system containing the necessary avionic components for system and software operation, commercially available components to support testing and monitoring, and special components which provide for comprehensive verification of system and software performance. This ISS system was designed and produced by COMPTEK Research, Inc. for the Warner Robins - Air Logistics Center (WR-ALC) prior to the development of the EEPROM/CPU upgrade.

This program was initiated by COMPTEK Research, Inc. at the suggestion of WR-ALC's Mr. Robert Smock (MMRRVA); Mr. Stephen E. Cooper and Mr. Donald R. Liedke of COMPTEK served as technical monitors. The Georgia Tech-Engineering Experiment Station (GT-EES) was involved because of its previous experience gained while designing the prototype EEPROM/CPU upgrade.

The work was performed at GT-EES under the general management of Mr. R. P. Zimmer, Director, Systems Engineering Laboratory, by members of the Electronic Support Measures Division under the supervision of Mr. L. D. Holland, Chief, and Mr. D. K. Plummer, Head, Surveillance Technology Branch. The GT-EES project director for this program was Mr. T. E. Tibbitts and principal technical contributors at GT-EES were Mr. J. T. Parish, Mr. C. K. Cole, Mr. R. K. Trussell, and Mr. H. L. Owen.

ABSTRACT

Due to the development of a new Central Processing Unit (CPU) for the AN/ALR-46, -46A, and -69 Radar Warning Receivers, it was necessary to upgrade the Integration Support Station (ISS) software and support equipment. This upgrade included development of a new computer control panel and a new interface to connect the CPU with the computer control panel.

This report contains the theory of operation and specifications for the new interface required to connect a modified AN/ALR-46, -46A, and -69 RWR to the new computer control panel to interface with the ISS.

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1.0 INTRODUCTION

1.1 Background

During the period of February 1980 - September 1981, the Georgia Tech Engineering Experiment Station (GT-EES) successfully designed and developed a prototype modification kit for the AN/ALR-46, -46A, and -69 Radar Warning Receivers (RWRs). This modification includes the redesign of the memory and central processing unit (CPU) and provides a growth capability for the future addition of a dual processor in operational units.

This CPU upgrade has made it necessary for certain ground support equipment to be modified so that the Warner Robins Air Logistics Center may continue to support all configurations of RWRs. Included in this ground support equipment is the ALR-46/69 RWR Integration Support Station (ISS) produced by COMPTEK Research, Inc. (CRI). This ISS includes a front panel display system which interfaces directly with the CPU and which therefore must be modified to operate with the new CPU.

1.2 Project Purpose

The purpose of this project was to aid COMPTEK Research, Inc. in identifying the changes necessary to interface the new CPU to the other ISS components in the current adapter subsystem, the data extraction subsystem, and the cabling system. The Georgia Tech-Engineering Experiment Station was to design, build and test a new CPU adapter capable of interfacing between a Fairchild 9445 microprocessor and the new computer control panel (designed by CRI). In addition, GT-EES was to supply any additional engineering support deemed necessary by CRI during the integration, testing and evaluation phase of the prototype modification.

1.3 Scope of this Report

This report contains the theory of operation and technical specifications for the front panel interface circuitry required to connect a Fairchild 9445 microprocessor CPU to the new computer control panel. The schematics in Appendix C will aid the reader in understanding the text material.

2.0 RELATED TECHNICAL MANUALS/DOCUMENTS

2.1 GT-EES Documents

"Developmental Design Data for a Field Reprogrammable Breadboard Modification Kit for the AN/ALR-46, -46A, -69 Radar Warning Receivers" Technical Report Under Contract No. F09603-78-G-4368-0014, September 1981 (Project A-2594)

3.0 THEORY OF OPERATION

3.1 System Description

The adapter joins together three units of the ISS. As shown in Figure 3-1, the adapter is the interface for communication between the RWR, the Data Extraction System (DX), and the Control Panel. The DX extracts information from the RWR through the adapter. The Control Panel connection gives the operator a way of operating the RWR. In fact, all control and data signals generated by the RWR pass through the adapter. Because of the key role played by the adapter in communications between the RWR and the Integration Support Station (ISS), the adapter is essential to testing an RWR on the ISS. Figure 3-2 shows the block diagram of the adapter.

The IB buffer serves as a window on the operations of the RWR processor. IB is a mnemonic for information bus, which is the primary operating bus of the RWR CPU. During normal operation of the RWR, any activity on this bus is communicated to the adapter through the IB buffer. Also, there are two instances in which information flows from the adapter through the IB buffer toward the CPU. When the CPU runs a program from the adapter's Automatic Program Load (APL) ROM memory, the CPU reads the program through the IB buffer. Secondly, codes for the operator's requests from his console to the RWR pass through the IB buffer. In this report, the definition of information includes addresses, instructions, operands, and data, all of which flow over the information bus.

The Address/Data (ADDAT) buffer drives the multiplexed information lines to the control panel. The information exchanged over the ADDAT bus includes RWR execution addresses, console request instruction codes, console switch settings, and data produced by RWR responses to console requests.

The Instruction Processor produces machine-coded console instructions for the RWR CPU. The response of the Instruction Processor follows the codes on the buffered ADDAT bus, which are produced by the operator at his console. The menu of instructions offered from the control panel is more extensive than the limited set of console operations built into the CPU microprocessor chip. To accommodate these more extensive console

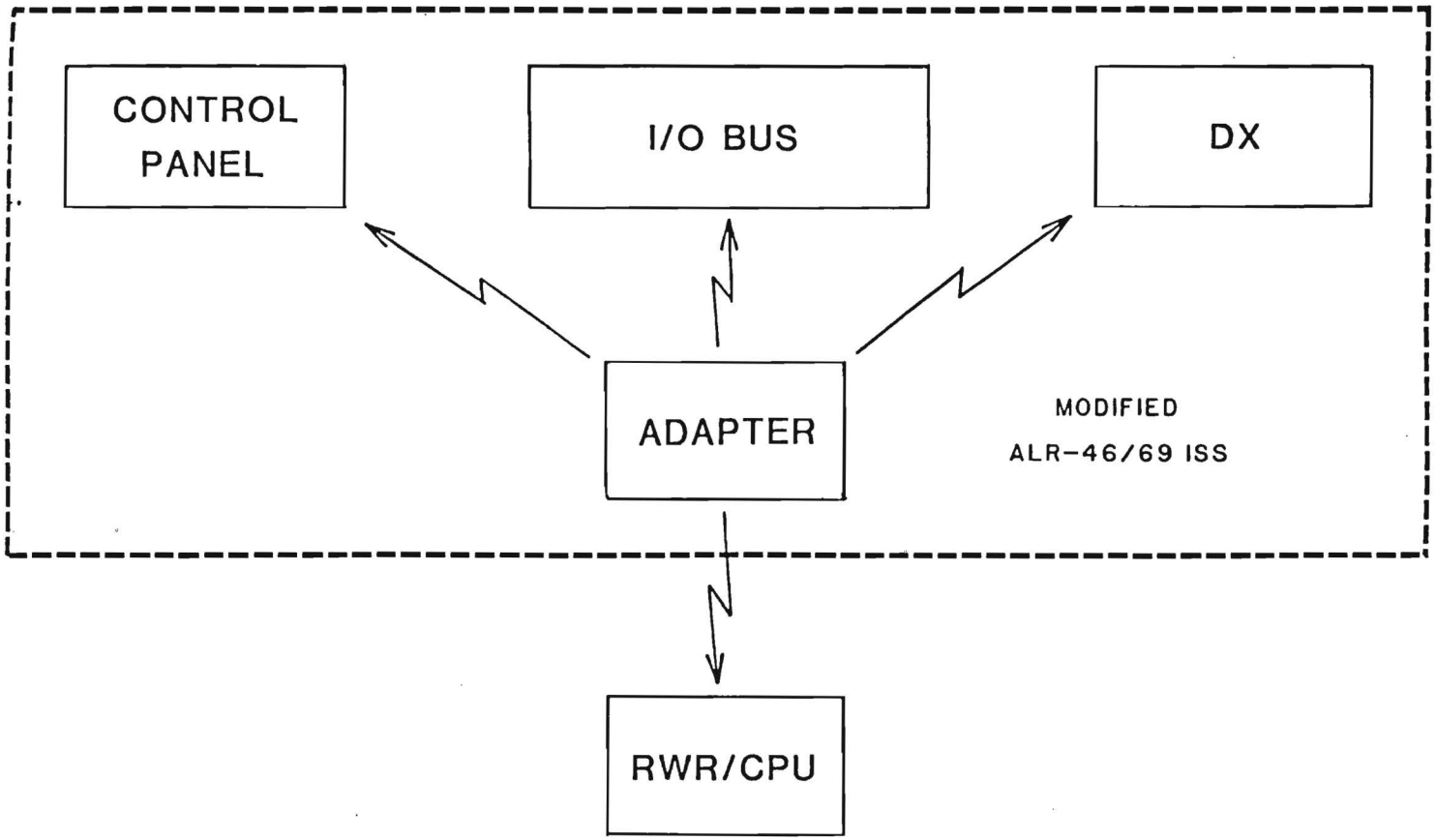


FIGURE 3-1 COMMUNICATIONS

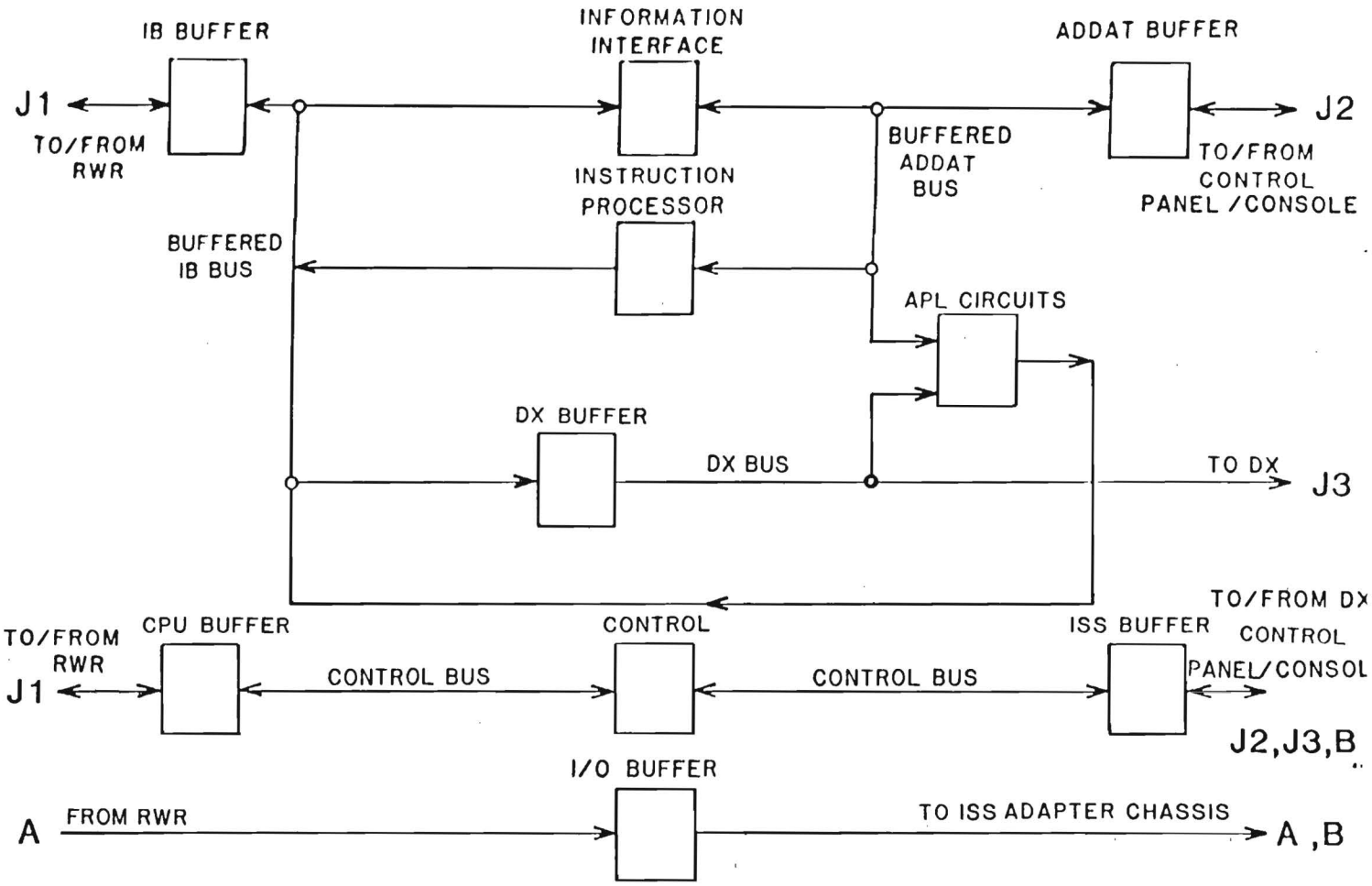


FIGURE 3-2 ADAPTER FUNCTIONAL BLOCK DIAGRAM

operations, two separate sets of the built-in CPU console intructions are automatically strung together by the adapter. Therefore, some control panel operations require the Instruction Processor to generate two instruction execution cycles in the CPU. After the first instruction has been performed, the Instruction Processor then interrupts the CPU a second time to deliver the second instruction code. The Instruction Processor contains an Instruction Code Synchronizer and an Instruction Encoder.

The Information Interface referees the exchange of information between the buffered IB bus and the buffered ADDAT bus. While the Instruction Processor is operating, the Information Interface is in a high impedance state. When the proper bus conditions are met, the interface transmits data from one bus to the other.

The DX buffer holds information from the buffered information bus for the DX. The DX buffer latches only the types of information that the DX extracts, and then signals the DX that the information is captured. As part of this function, the DX buffer demultiplexes the addresses and data it presents to the DX circuitry.

The APL circuits load a stored program into the CPU. This program must use less than 2K words of memory. Optimally, the program stored in the APL circuitry should also be relocatable, because the console operator maps the stored program into the RWR CPU memory while running the program. In fact, the operator can place the APL program anywhere in memory, and it will be accessed by a normal CPU-read of those memory locations indicated by the operator at the start of the task. The physical memory in the RWR CPU is still writable, so that CPU-write cycles accessing the memory occupied by the APL program correctly modify the RWR physical memory. However, a read-memory cycle on the locations in use by the APL circuits produces information from the APL program. The APL circuits become inactive when any instruction is fetched outside the APL's 2K space or when they are reset by the front panel switch. The APL circuitry can be mapped to any one of the 2K boundaries in memory. Since the APL circuitry does not disturb the physical memory in the RWR CPU, and since the APL circuitry is automatically selected by normal CPU operations, the APL program always resides in a virtual memory segment which is relocatable by the console operator.

The I/O Data Buffer posts all I/O bus actions by the RWR CPU to the ISS adapter chassis "A" and "B" connectors (Figure 3-3). The I/O Control Buffer monitors the device select and strobe lines for the I/O bus control signals to transmit this data. The I/O information from the CPU IB is latched into a data register on the adapter; any data moved by the RWR will be reflected on the ISS adapter chassis "B" bus.

The I/O control Programmable Array Logic (PAL) manages the operations of the adapter, linking together the ISS Data Extraction (DX) circuit, the console, and the RWR. The control PAL circuitry includes a console request latch that interrupts the processor, a run monitor that senses activity in the CPU, a strobe timer, and a fetch-state latch. The strobe timer and fetch-state latch generate special signals needed by the ISS DX. In addition, numerous other signals are generated by the PAL logic arrays (described later in the report).

The bus control signal flow is shown in Figure 3-4. This diagram takes on additional importance because so much of the adapter circuitry operates in synchronism with the RWR CPU. In fact, all of the inputs from the other two arms of the adapter shown in Figure 3-1 (DX and the control panel) are level sensitive. A description of the individual circuits shown is provided in the section on PAL programming. The instruction processor and APL circuits must be actuated by CPU bus control signals. The direction of information flow through the IB buffer, ADDAT buffer, and information interface is partly determined by the CPU bus control lines.

Figure 3-5 shows the flow of CPU timing signals into the adapter. All of the strobes produced in the adapter are derived from these timing signals. In fact, APL ROM memory access cycle timing as well as the states of the instruction code synchronizer directly follow the timing signals produced by the CPU. The control PALs are combinatorial logic circuits, but the strobes produced by these PALs use the CPU timing signals.

The adapter implements all of the console requests produced by the ISS by means of the console request feature of the RWR CPU. The various console request sources are shown in Figure 3-6. The Master/Slave feature requires a jumper selection on the adapter. Each adapter is capable of generating either the slave adapter's console request or the master adapter's response, and jumpers E1 and E2 determine which is active. PAL U7 processes

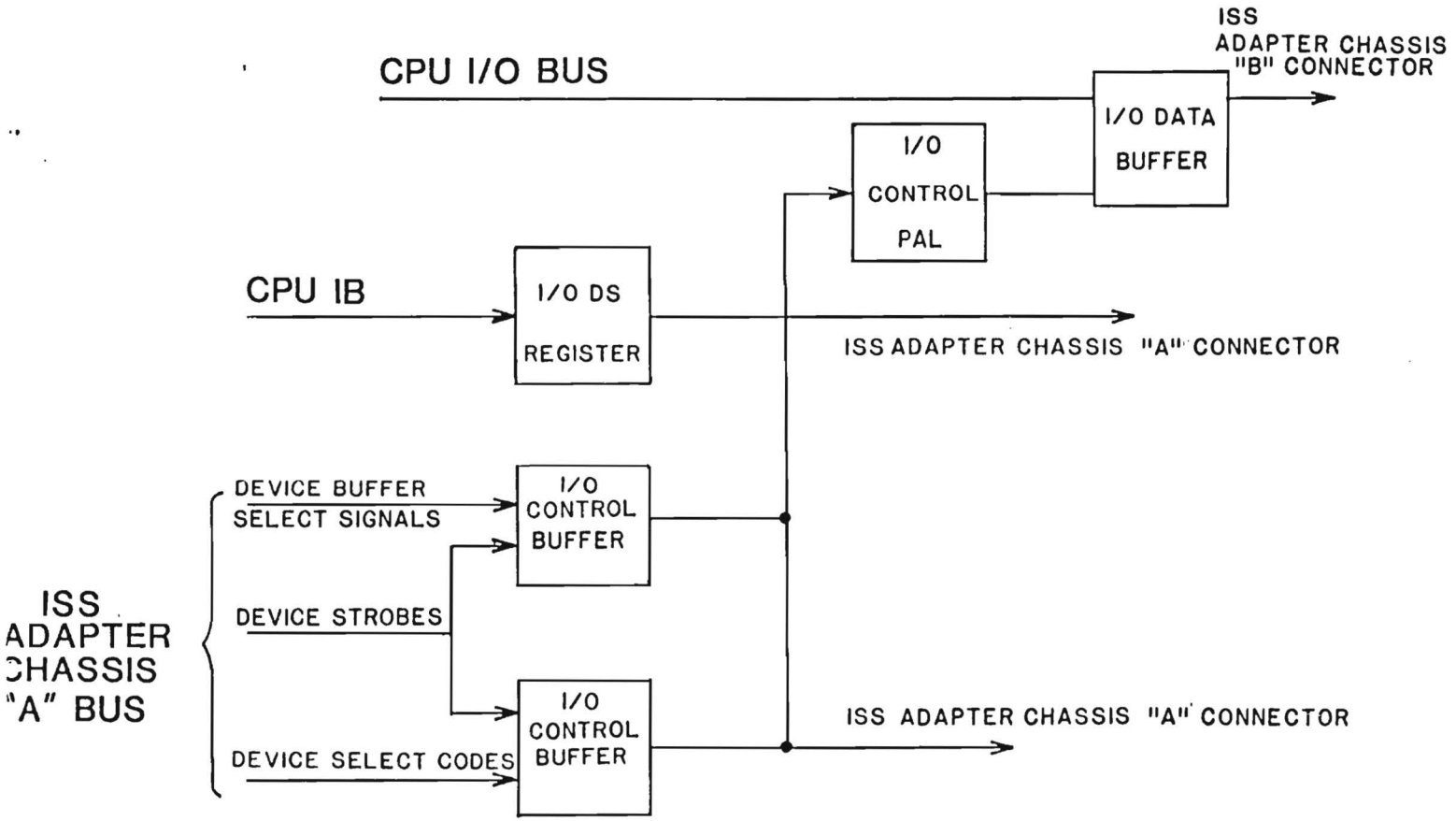


FIGURE 3-3 I/O PROCESSING

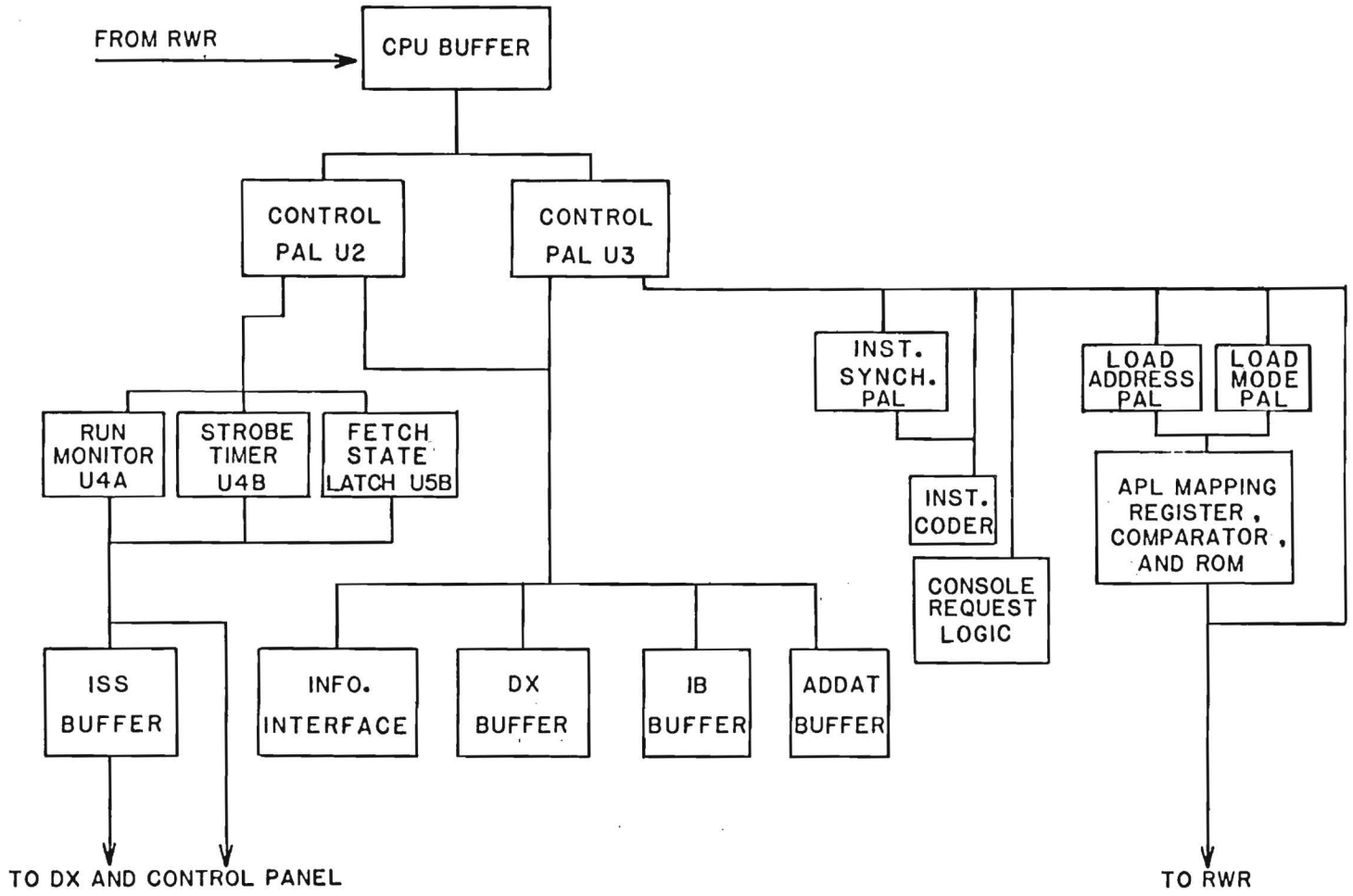


FIGURE 3-4 BUS CONTROL PROPAGATION

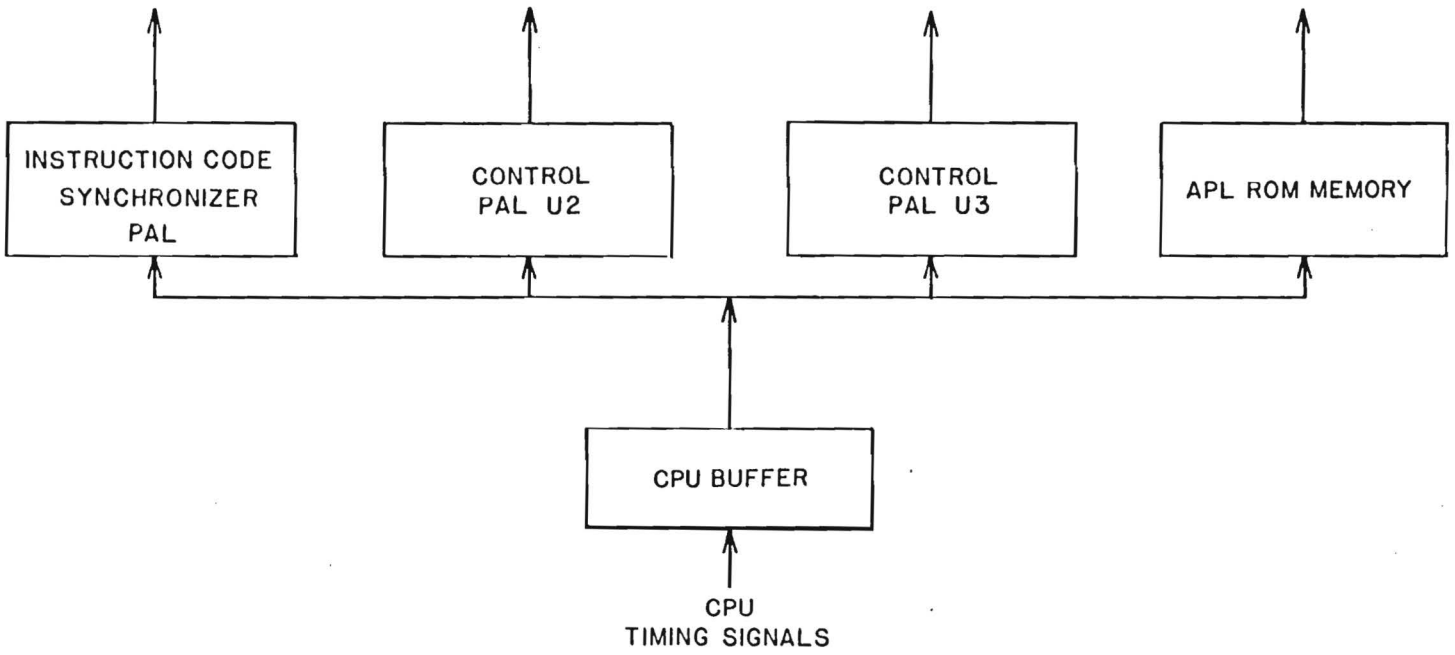


FIGURE 3-5 TIMING SIGNALS FROM THE RWR

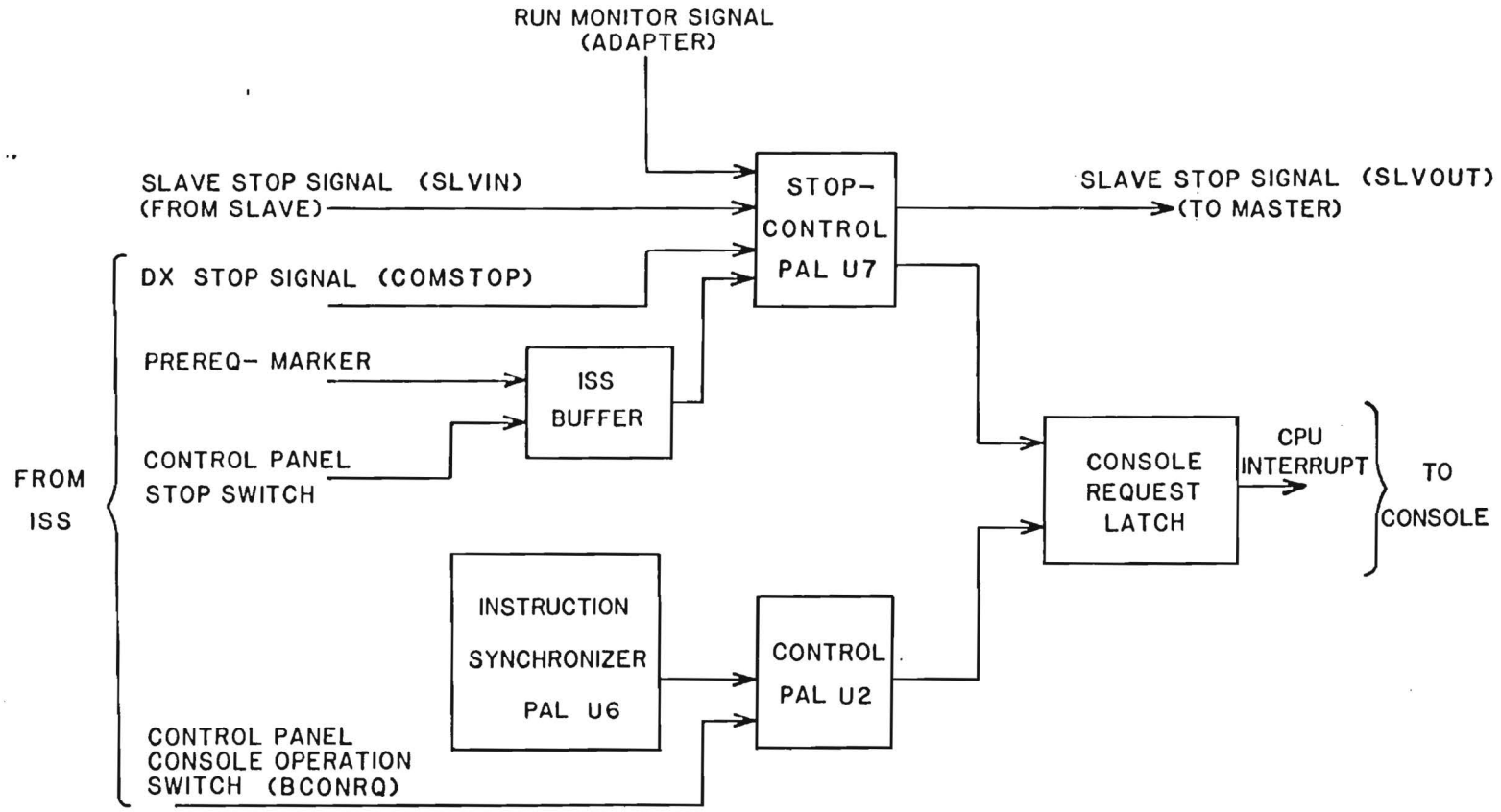


FIGURE 3-6 CONSOLE REQUEST LOGIC

all of the stop signals. This PAL also generates the slave requests to the master adapter.

3.2 PAL Programming

This section of the report describes the logic functions implemented by the PALs. Each function is treated individually. The overall view of the functions interacting with each other is given in Section 3.3. The goal in this section is to give a detailed description of the conditions necessary for each signal to be active. When the signal is low true, that is, when asserting the signal produces a ground on the line, a minus sign follows the name of the signal. Conversely, a plus sign follows for high true signals. Many of the signals, however, are derived from information lines, and these signals are shown simply as a mnemonic. These aids to the reader make interpretation of the logic functions easier, and their use clarifies the relationships among the signals in the adapter. This section serves also as a useful aid to technicians diagnosing failures within an adapter; however, the broader view of the next section facilitates locating the trouble.

Designing with PALs is similar to designing with AND-OR-INVERT (AOI) gates. A PAL is essentially a field of programmable fuses in the AND plane of a gate array. The OR terms of the array are committed, and each signal is inverted at the output pin. The flexibility of the gate arrays used in this design stems from the feedback terms available on the chip. This makes state machines possible that have no external next-state feedback connections. Internal feedback also makes multiple level logic more reliable and faster.

3.2.1 PAL U2

The PAL U2 (Figures 3-7A to 3-7C) generates signals that affect each of the interfaces connected to the adapter.

Figure 3-7A: DXR- and DXW- are the read and write strobes for the DX. Without an EEPROM/CPU plugged into the adapter, DXEN- (J1-2) high holds the inverters (that drive DXR- and DXW) in their high impedance state. With an EEPROM/CPU plugged in, DXR- asserted low indicates that a CPU memory read is taking place. DXW- asserted low indicates that a CPU memory write is taking place. The buffered bus control signals BW

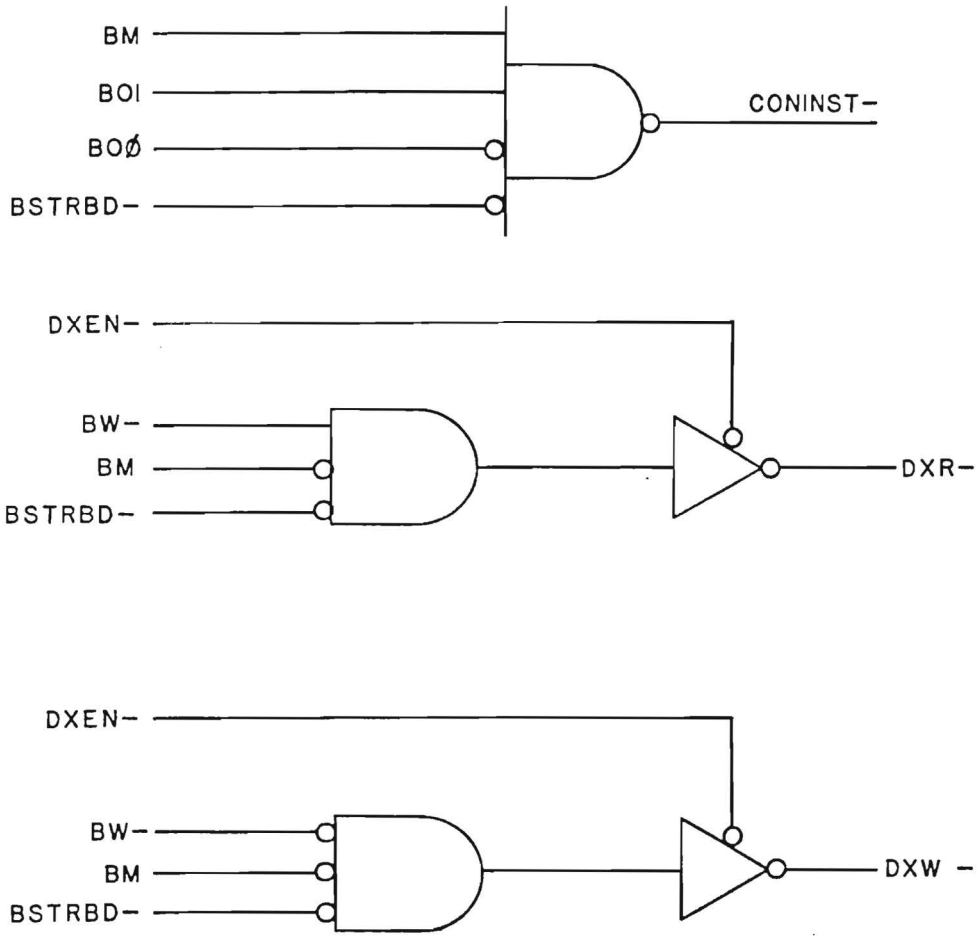


FIGURE 3-7A PAL U2

and BM become valid during the first microstate of the RWR CPU. In fact, these signals are derived from the read/write and memory control lines of the CPU. The BSTRBD-timing strobe indicates that data on the CPU information bus is valid. DXR- is active when BW- is high, whereas DXW is active when BW- is asserted low.

PAL U2 asserts CONINST- low when the RWR CPU is reading a console instruction code. PAL U2 monitors the bus control lines for a specific state, which is BM high, BO1 high, and BO0 low; then, when the RWR CPU indicates that it expects a valid instruction code on the information bus, PAL U2 uses CONINST to strobe circuitry on both the adapter and the control panel.

Figure 3-7B: Two more signals generated by PAL U2, CBLOAD- and READS- control the exchange of data between the RWR CPU and the control panel. Console instruction code-reads are often followed by control panel data-reads or-writes. The bus control lines have nearly the same state for both of these operations, but the two operations are distinguished by the sense of the BW- signal. When the RWR CPU signal BW- is low, it is writing data to the control panel displays, and PAL U2 uses CBLOAD-to strobe the control panel circuitry. When BW- is high, it is reading the control panel switches, and PAL U2 uses READS- to strobe the data onto the information bus. To accommodate these transfers, PAL U2 generates a third signal, DIR-, to control the direction of information flow through the Information Interface and the ADDAT Data Buffer.

Figure 3-7C: The last signal generated by PAL U2, REQCK-, is a normally high signal connected to the clock line of the console interrupt request latch. When a console instruction is required, a pulse on REQCK changes the state of the console interrupt request latch to notify the RWR CPU that a console instruction is pending. Either PAL U6 signal SPEC- or Control Panel signal BCONRQ+ acts to drive REQCK+ high, although the PAL only recognizes SPEC- if it receives the timing signal STRBA- from the RWR CPU.

3.2.2 PAL U3

PAL U3 (Figures 3-8A to 3-8D) also generates signals to communicate with each of the interfaces connected to the adapter.

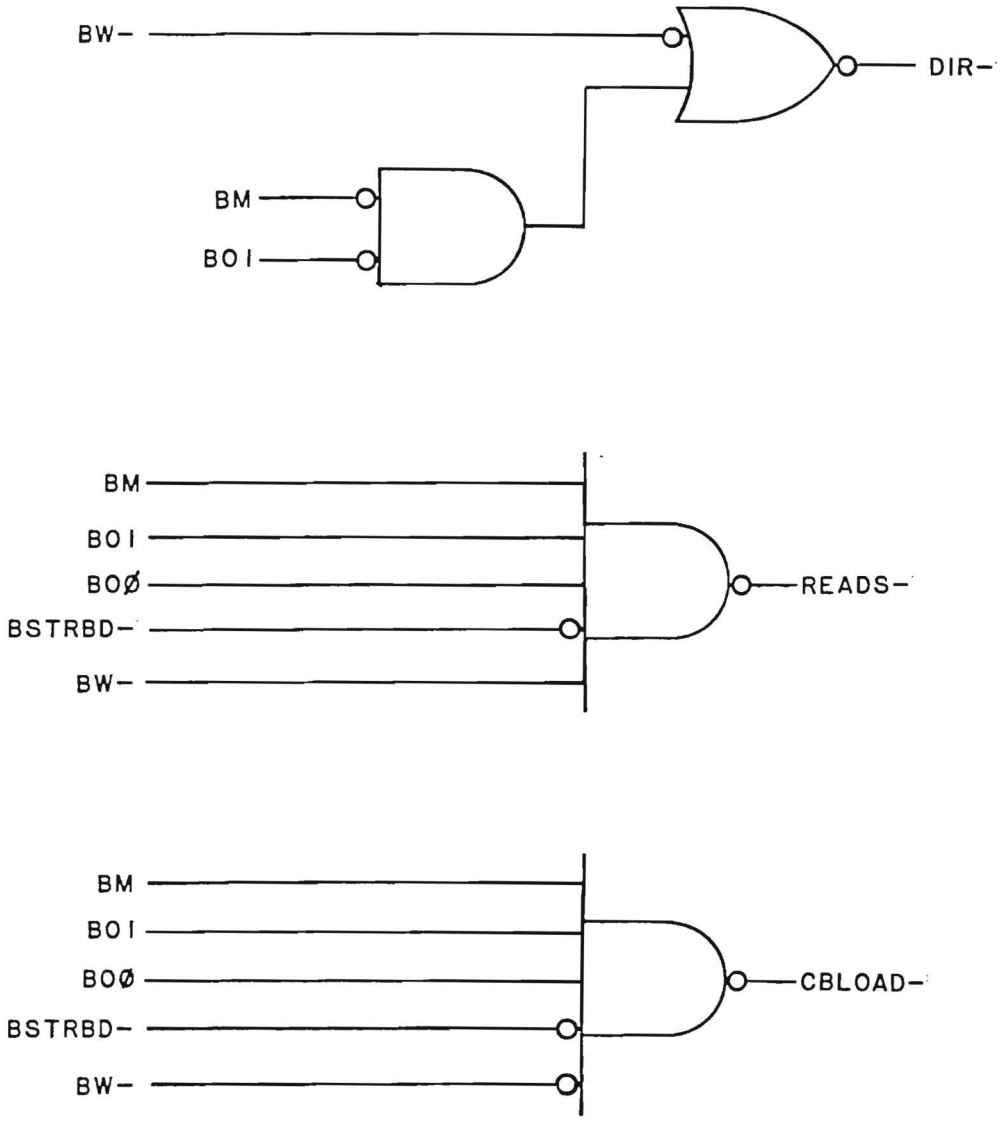


FIGURE 3-7B PAL U2

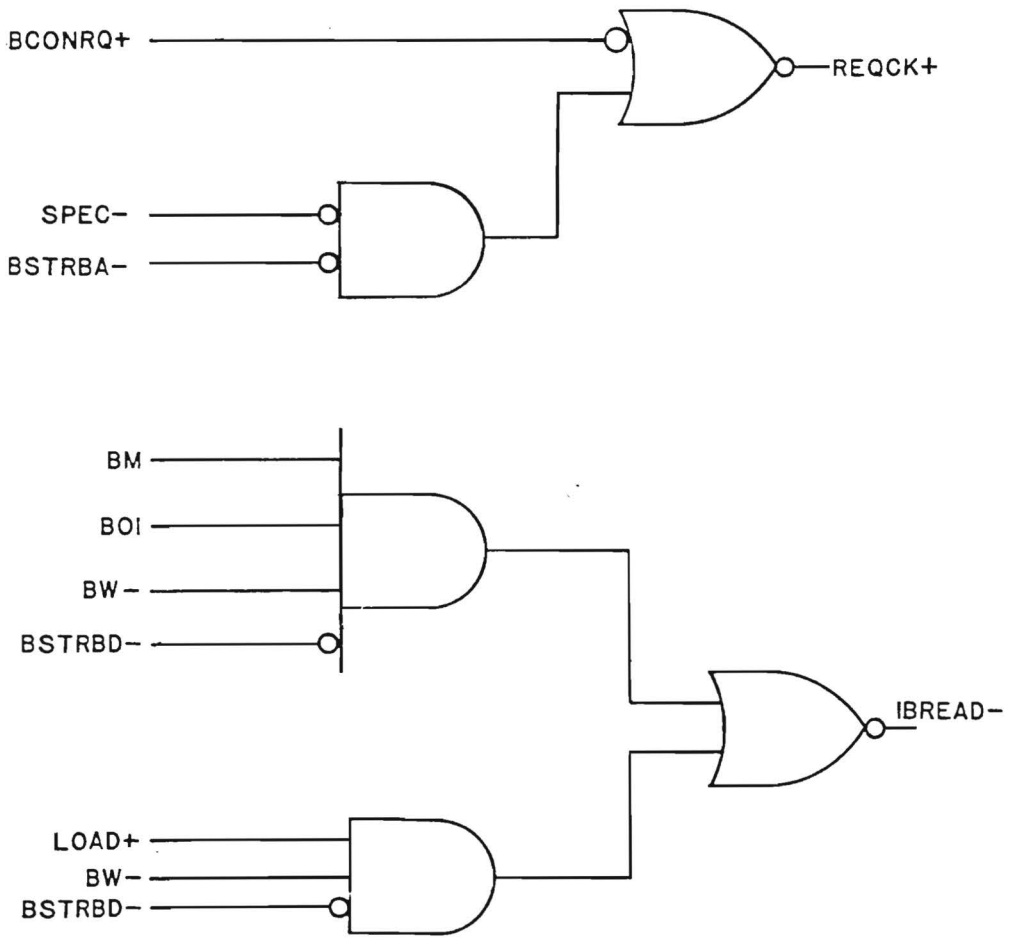


FIGURE 3-7C PAL U2

Figure 3-8A: DTG- fires the strobe timer that insures capture of data on the information bus by the DX buffer. When the RWR CPU accesses data in its memory space, the CPU asserts BM. The CPU strobe BSTRBD- will then fire the adapter strobe timer.

PAL U3 signal CLEAR- moves the APL ROM-stored program out of the RWR CPU's memory space. PAL U3 asserts CLEAR- only when any instruction is fetched outside the 2K APL address space or when the adapter circuitry is reset by the console operator. The input signal LOAD+ (U21-6) is high during the execution of an APL ROM instruction. When the instruction is completed, LOAD+ falls.

Figure 3-8B: PAL U3 signal FETCH- is only active when an EEPROM CPU is being used in the RWR. DXEN- holds the inverter that drives the PAL output pin in a high impedance state if an EEPROM CPU is not being used. If DXEN- is low, then RWR CPU instruction-fetches and direct-operand-accesses assert the FETCH- line. FETCH- updates the address display on the control panel and clocks latch U5B on the adapter.

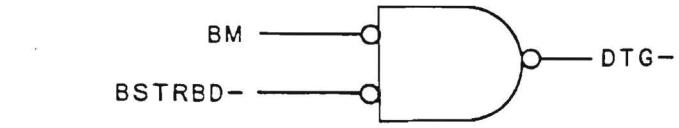
Figure 3-8C: PAL U3 signal DCH- indicates that a data channel cycle is in progress in the RWR and is used to drive the DCH light on the front panel. This signal is generated when the condition BM high, BO1 low, and BOØ high exist on the control lines.

PAL U3 signal MADD+ latches the address of each RWR CPU memory cycle into the DX Buffer.

PAL U3 signal RUNSTRB- re-triggers one-shot U4A as long as activity occurs in the RWR CPU. PAL U3 looks for instruction-fetches and data-channel-cycles as evidence of activity in the RWR CPU.

Figure 3-8D: PAL U3 signal BADDATE- enables the ADDAT Buffer whenever information must be exchanged between the RWR CPU and the Control Panel. PAL U3 monitors the RWR CPU bus control lines for console operations and instruction fetches. PAL U3 enables the ADDAT Buffer during instruction fetches while the RWR CPU address is valid, to update the Control Panel address display. The PAL enables the ADDAT buffer again during RWR CPU console operations to allow an exchange of information with the Control Panel.

PAL U3 signal MEMLD- disables the physical memory in the RWR CPU when it is appropriate to use the APL ROM program stored in the adapter's APL circuitry. LOAD+ is active when an APL instruction is executed.



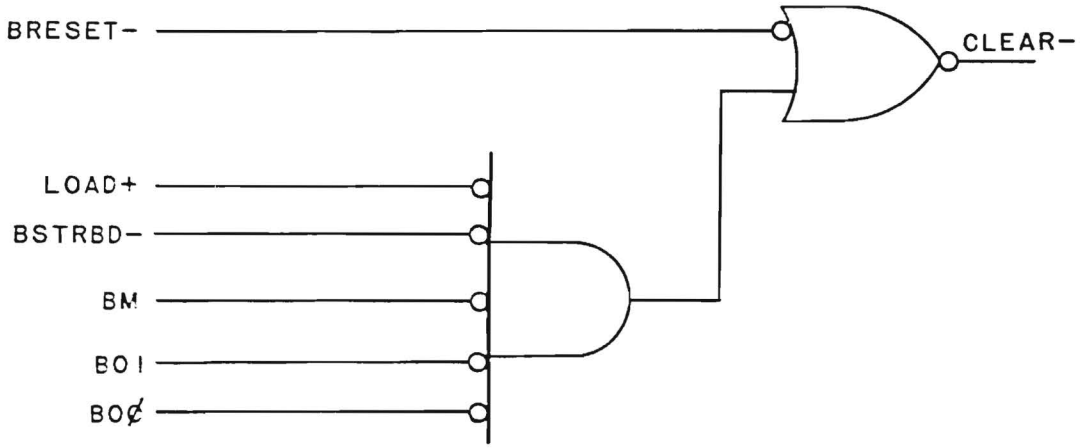


FIGURE 3-8A PAL U3

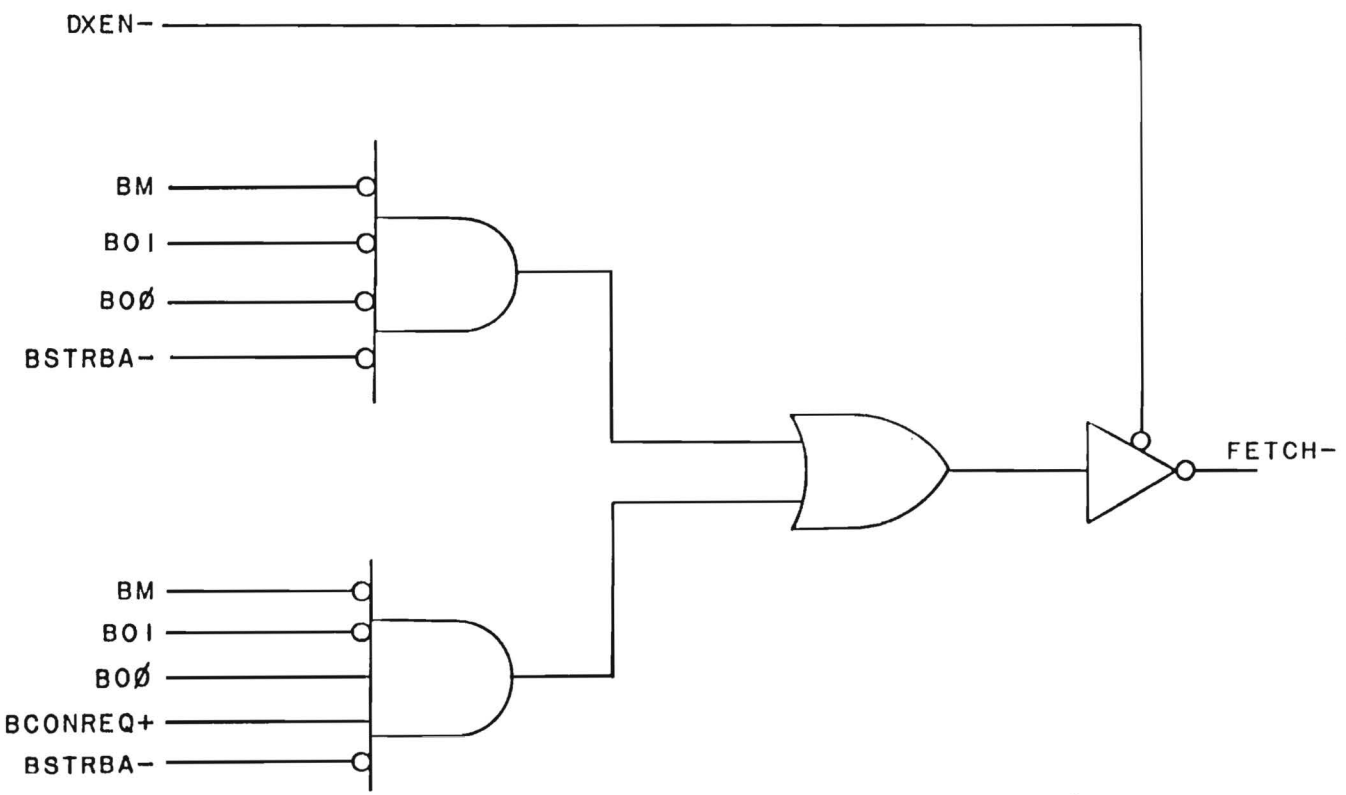


FIGURE 3-8B PAL U3

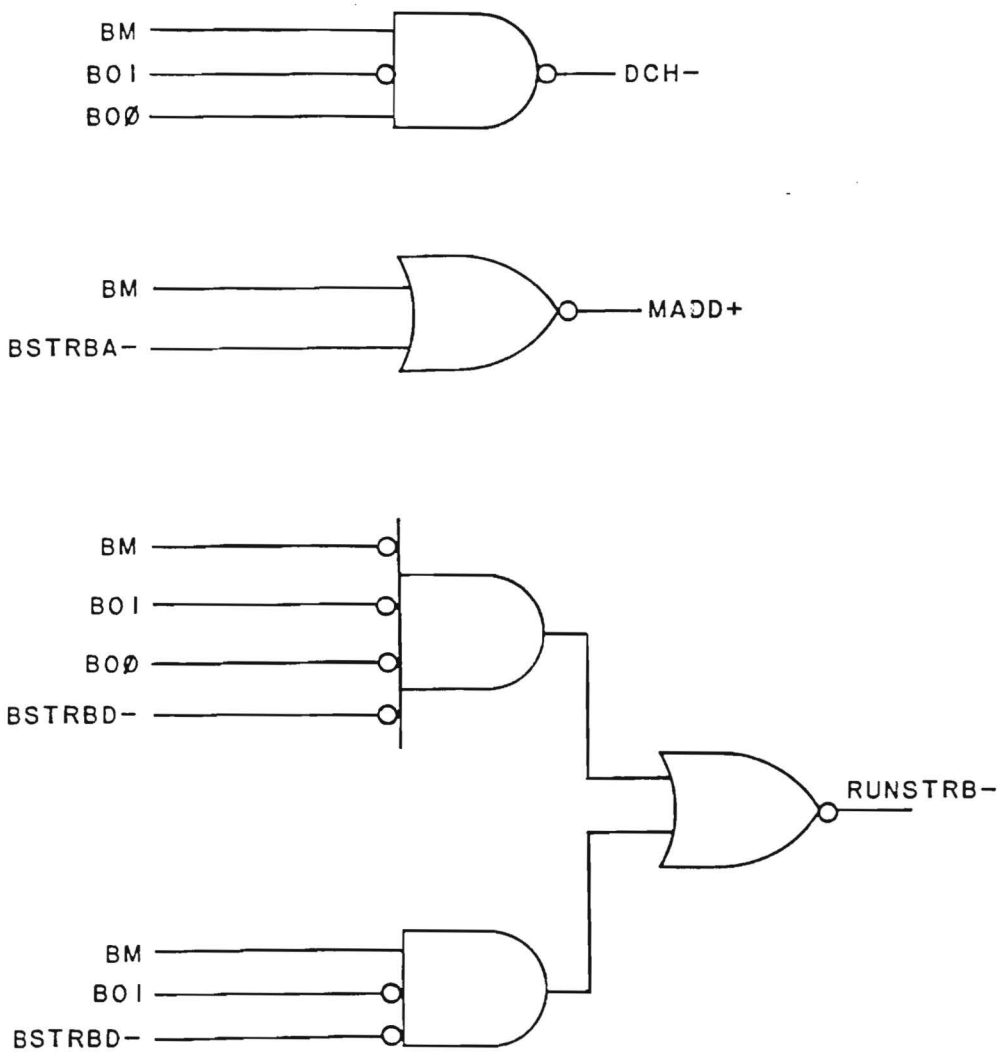
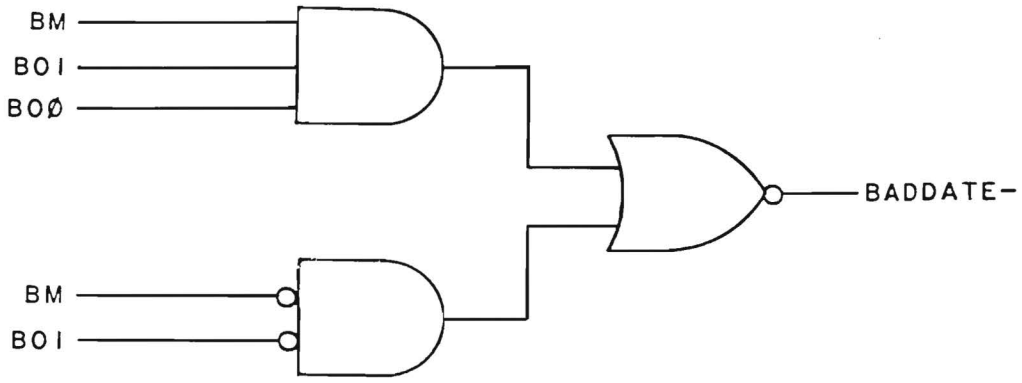


FIGURE 3-8C PAL U3



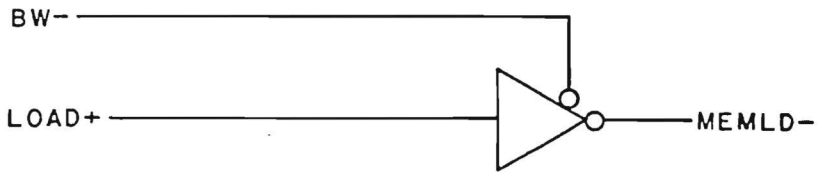


FIGURE 3-8D PAL U3

3.2.3 PAL U6

PAL U6 (Figures 3-9A to 3-9D) is a registered PAL, which means that the PAL operates synchronously with the signal applied to its clock input. All of the output signals of the PAL change state on the positive-going edge of the clock signal. This PAL receives its clock from the the RWR CPU timing strobe BSTRBD-. The signal DEL- is only used internally by the PAL. DEL- is active during an intermediate state of the PAL, and its availability on pin 14 facilitates troubleshooting.

Figure 3-9A: PAL U6 signal SPEC- indicates that a console code has appeared on the ADDAT bus which requires two console instruction cycles in the RWR CPU. Three feedback terms internal to the PAL hold SPEC- active during the completion of the two console instruction cycles. The SPEC- positive feedback input will hold SPEC- asserted as long as the RWR CPU does not access memory. In addition, CONT- and HALT-, which are also PAL U6 outputs, hold SPEC- asserted while CONT- and HALT- are high.

Figure 3-9B: PAL U6 signal DEL- is asserted during an RWR CPU console instruction read. DEL- asserted low encodes an intermediate state between the first and second console instruction codes produced by the adapter.

Figure 3-9C: The PAL U6 signal CONT- is asserted when the second RWR console instruction is a continue. CONT- is asserted after SPEC-and DEL- are driven low. A feedback term holds CONT- low during the next console instruction read.

PAL U6 signal HALT- is asserted when the second RWR console instruction is a halt. For instance, manual execution of a single instruction from the control panel requires the adapter to issue a CONT code followed by a HALT. HALT- is asserted if DEL- is not driven low, and SPEC- indicates that two instructions are required.

Figure 3-9D: PAL U6 signal LATCH+ clocks latch U20. This latch determines the block of physical memory assigned to the APL ROM. The line is driven low when the code for an APL load appears on the ADDAT bus. The LATCH+ signal remains low for one CPU instruction cycle, then LATCH+ is again asserted high. The positive going edge of LATCH+ will occur as the mapping address from the control panel appears on the ADDAT bus.

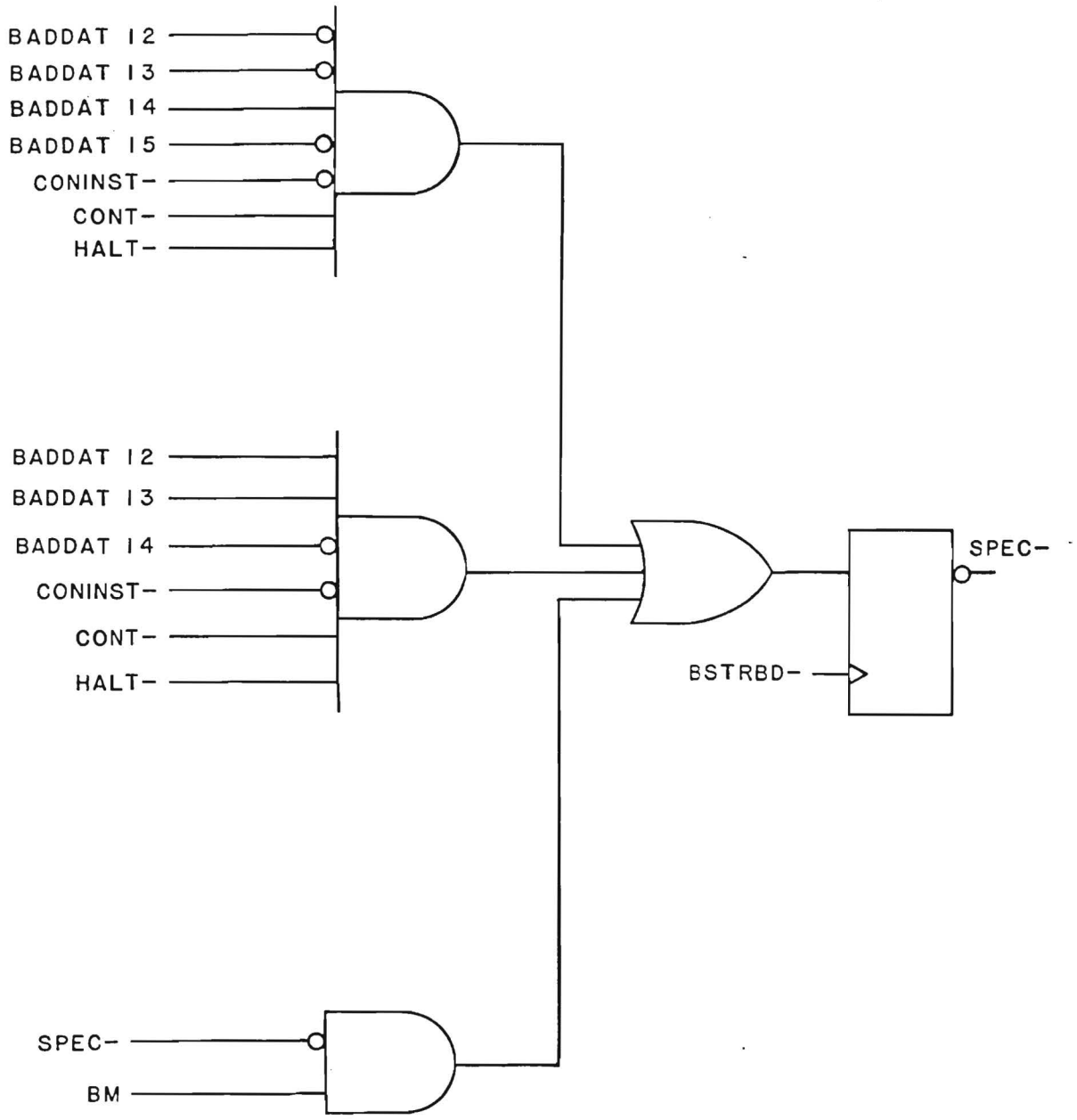


FIGURE 3-9A PAL U6

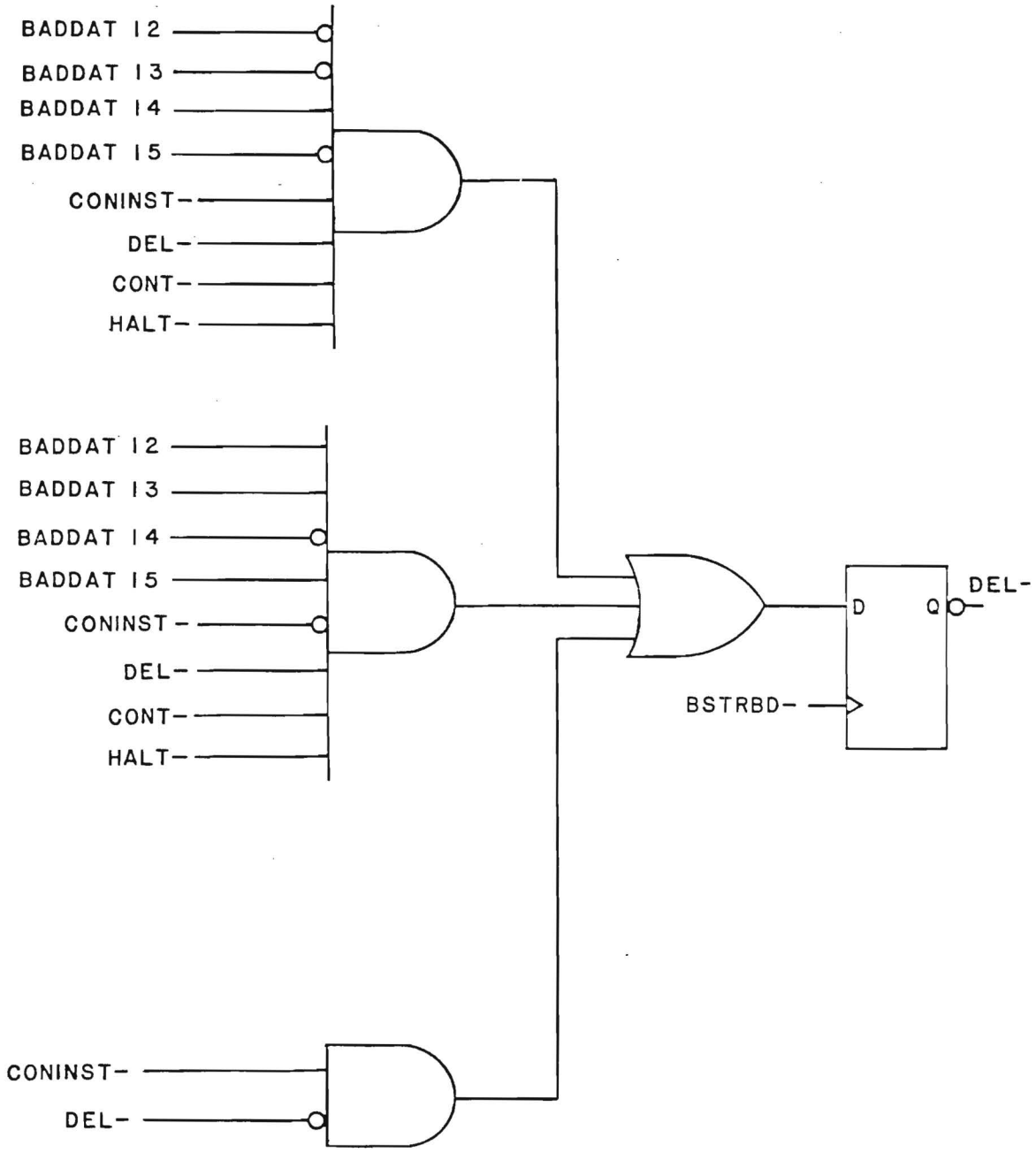


FIGURE 3-9B PAL U6

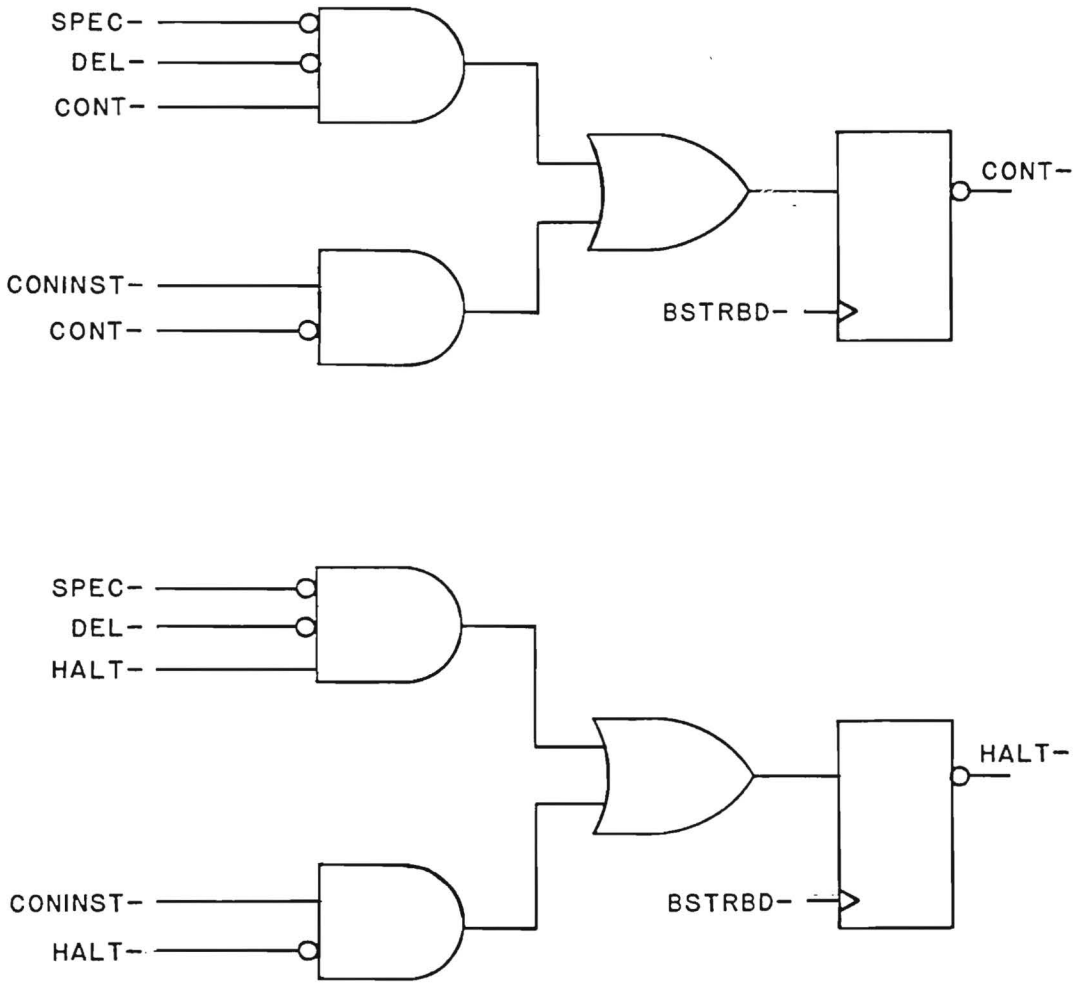


FIGURE 3-9C PAL U6

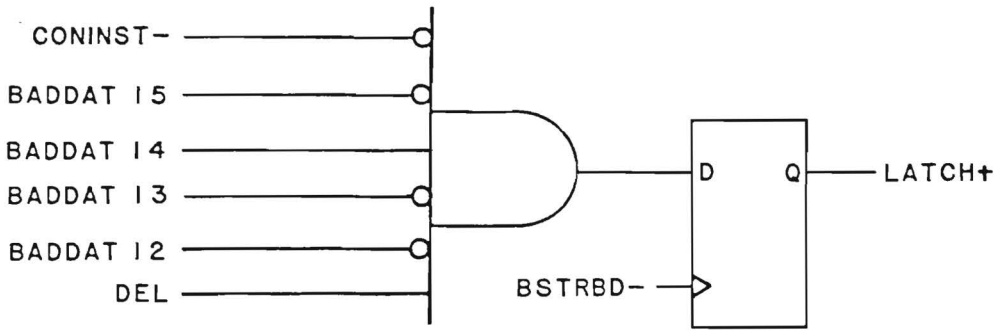


FIGURE 3-9D PAL U6

3.2.4 PAL U9

PAL U9 (Figures 3-10A to 3-10F) is a combinational circuit that operates on the console operation codes on the ADDAT bus and the two signals CONT- and HALT- from PAL U6. PAL U9 is only active during RWR CPU console code-reads, and is used to translate the codes from the Control Panel and PAL U6 into machine code for the RWR CPU. The two signals CONT- and HALT override the codes appearing on the ADDAT bus (See Figures 3-10A to 3-10E).

Figure 3-10F: PAL U9 signal COMPARE+ limits the operation of the APL circuits to RWR CPU memory accesses. COMPARE+ also restricts the APL circuitry from operating, after the adapter is reset, until a load operation occurs. The input APLEN- will be low after a reset until the operator at the control panel initiates a load. APLEN will hold COMPARE+ low until the RWR CPU acknowledges the load operation interrupt, and strobes the proper address into latch U20.

3.2.5 PAL U7

PAL U7 (Figures 3-11A to 3-11C) allows the two CPUs in the RWR to be operated independently. SLVIN and SLVOUT prevent a deadlock from occurring because the two CPUs are being operated in an unusual mode. These signals allow the Slave CPU to create an instruction cycle in the Master CPU so that the Slave CPU can request access to the I/O bus.

Figure 3-11A: PAL U7 signal SLVOUT indicates that the RWR CPU is executing a data channel cycle. Harmless glitches on this line due to skews in the bus control signals do not affect the adapter circuitry.

The register code buffer function is implemented in this same PAL. During RWR CPU console instruction reads, the register code from the ADDAT bus will be driven directly onto the information bus in the adapter. The register codes do not require translation by PAL U9.

The run state logic is also incorporated into this PAL. The run state logic signal STOPREQ- provides a means of halting the RWR CPU. STOPREQ- affects the Console Request Latch U5A. The adapter allows three different methods of stopping execution in the RWR CPU. The Control Panel stop switch asserts the input BSTOP+, which is recognized by the PAL only during instruction fetches and direct operand fetches. The ISS controls COMSTOP+, which is also only recognized by the PAL during instruction fetches

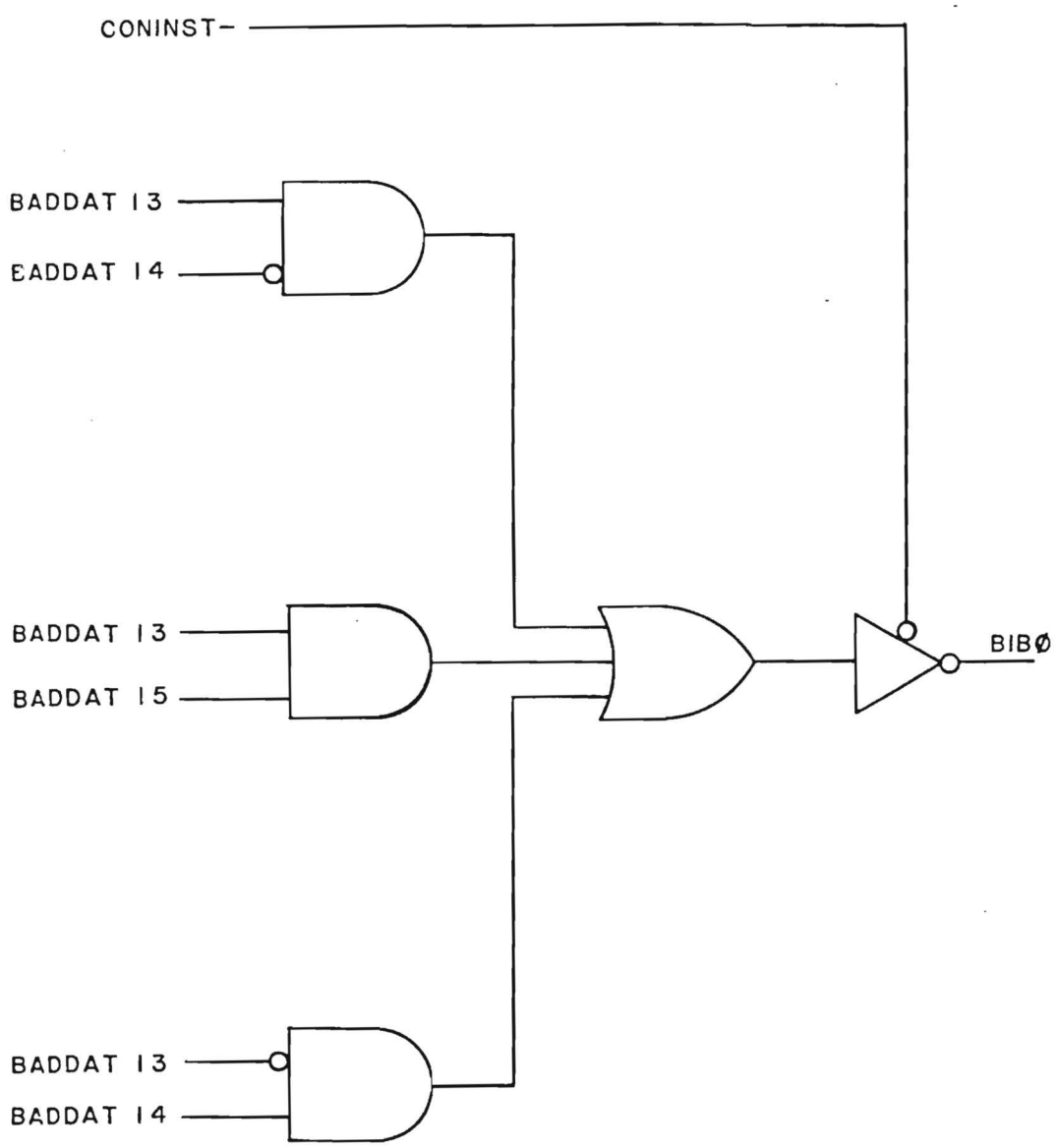


FIGURE 3-10A PAL U9

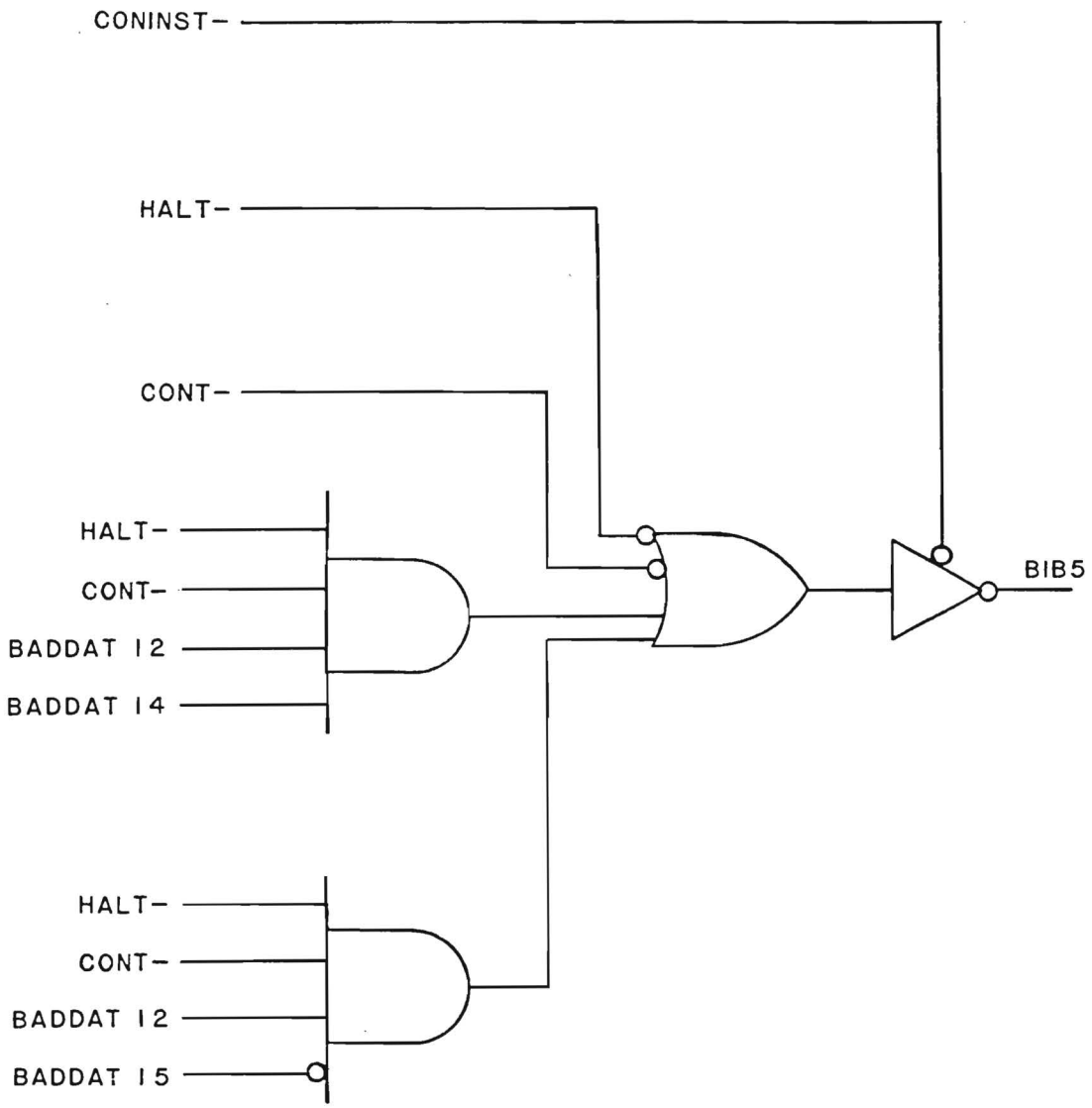


FIGURE 3-10B PAL U9

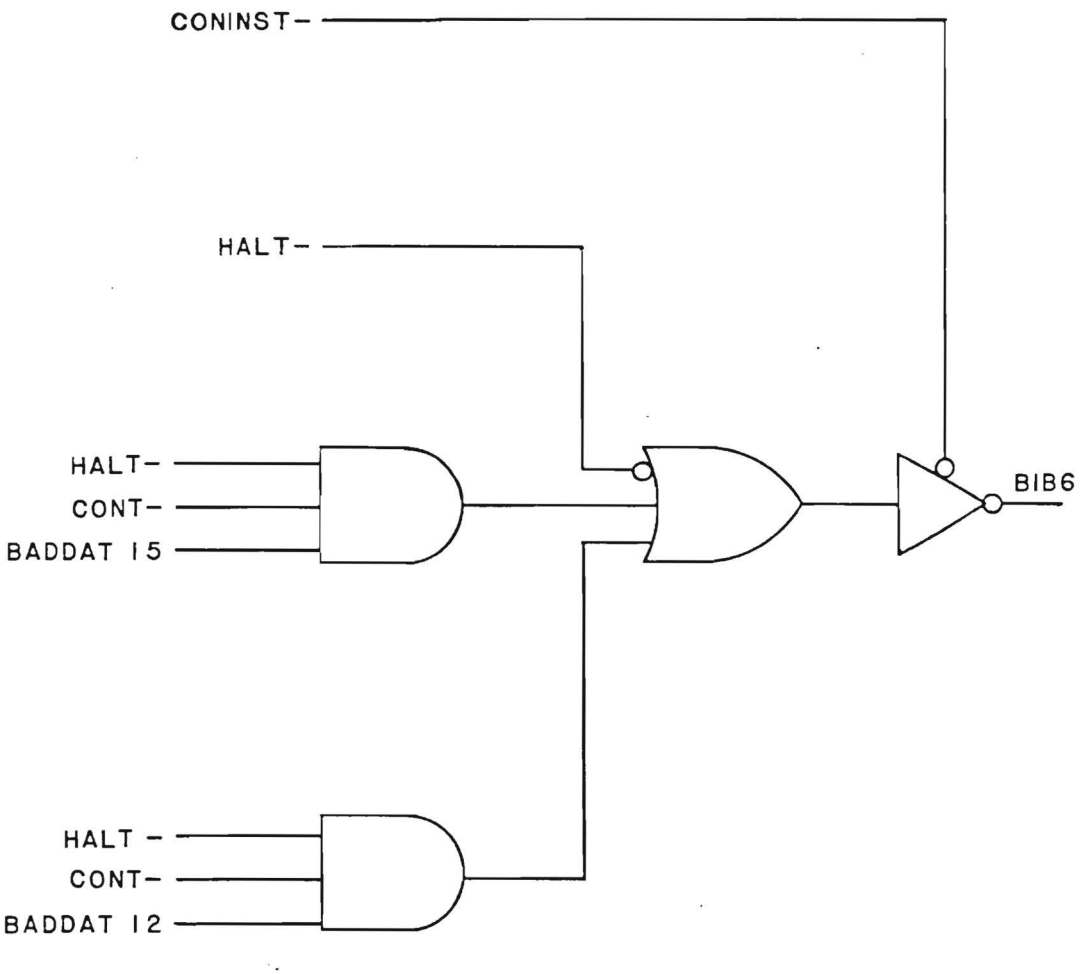


FIGURE 3-10C PAL U9

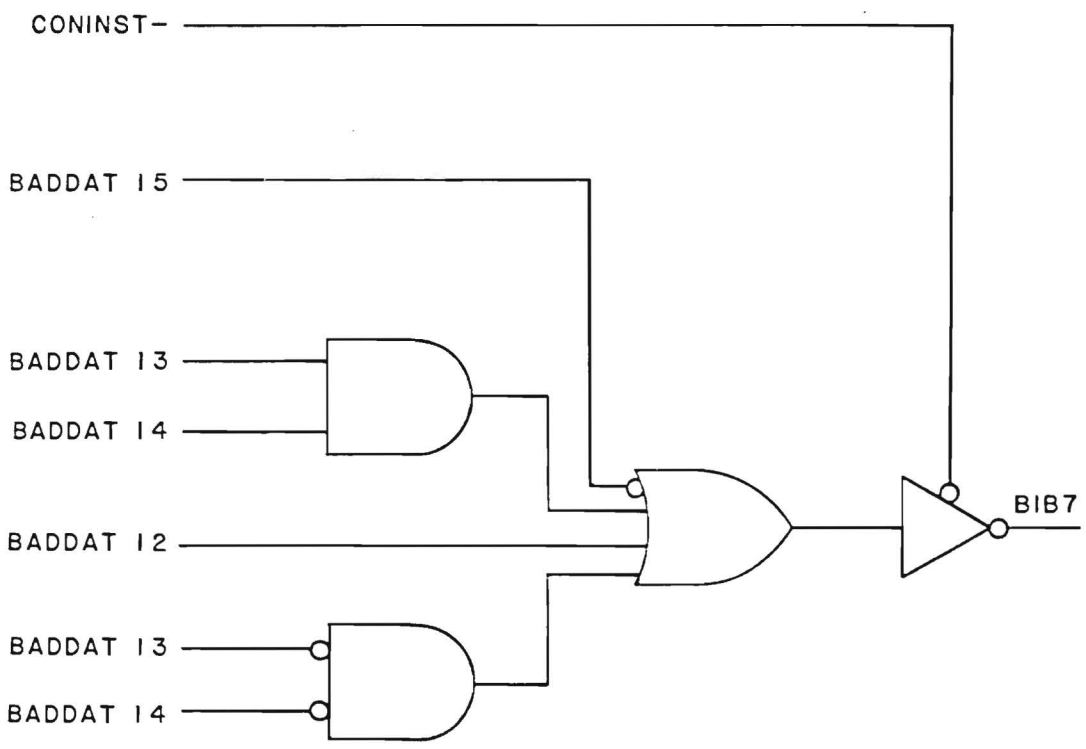


FIGURE 3-10D PAL U9

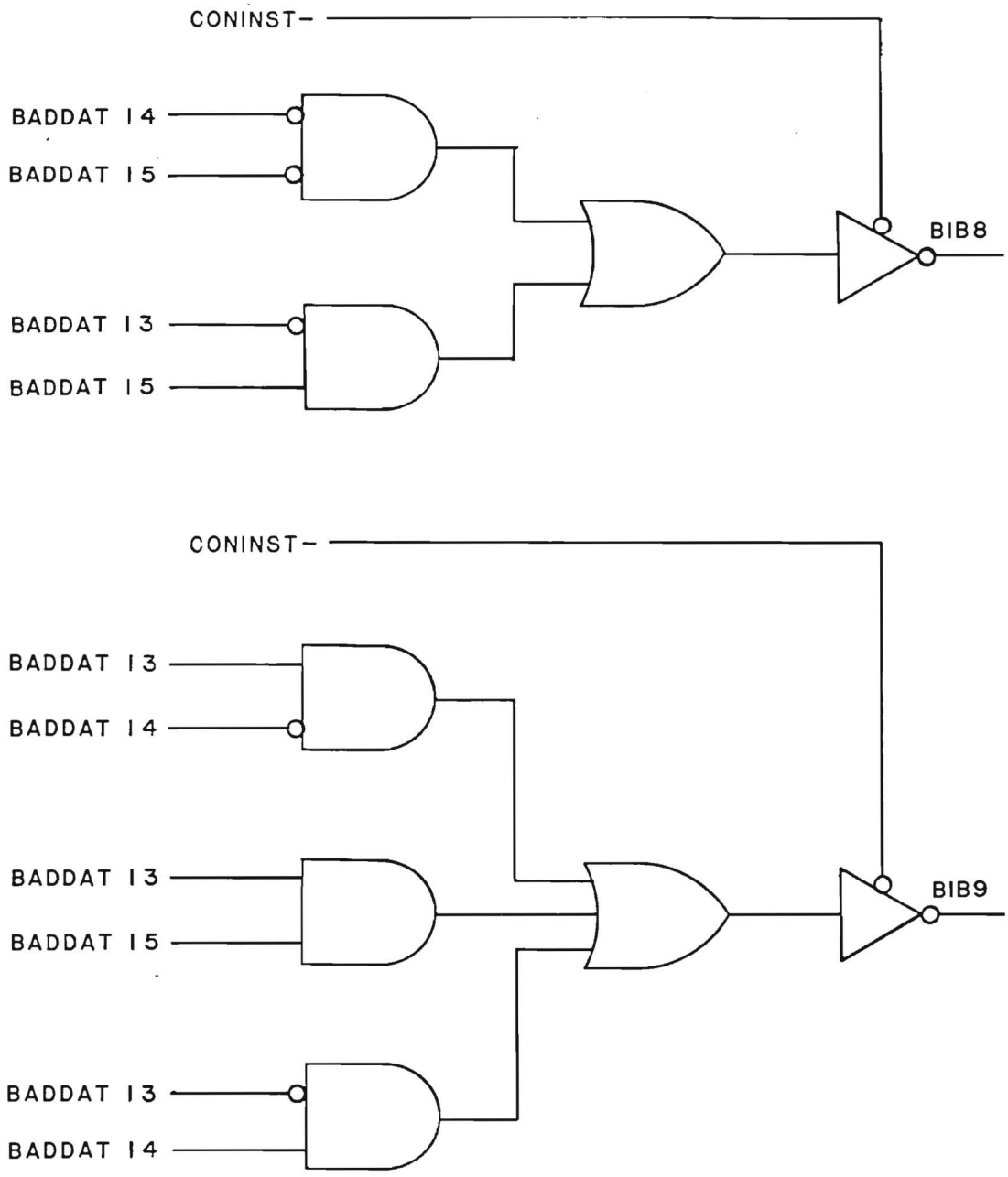


FIGURE 3-10E PAL U9

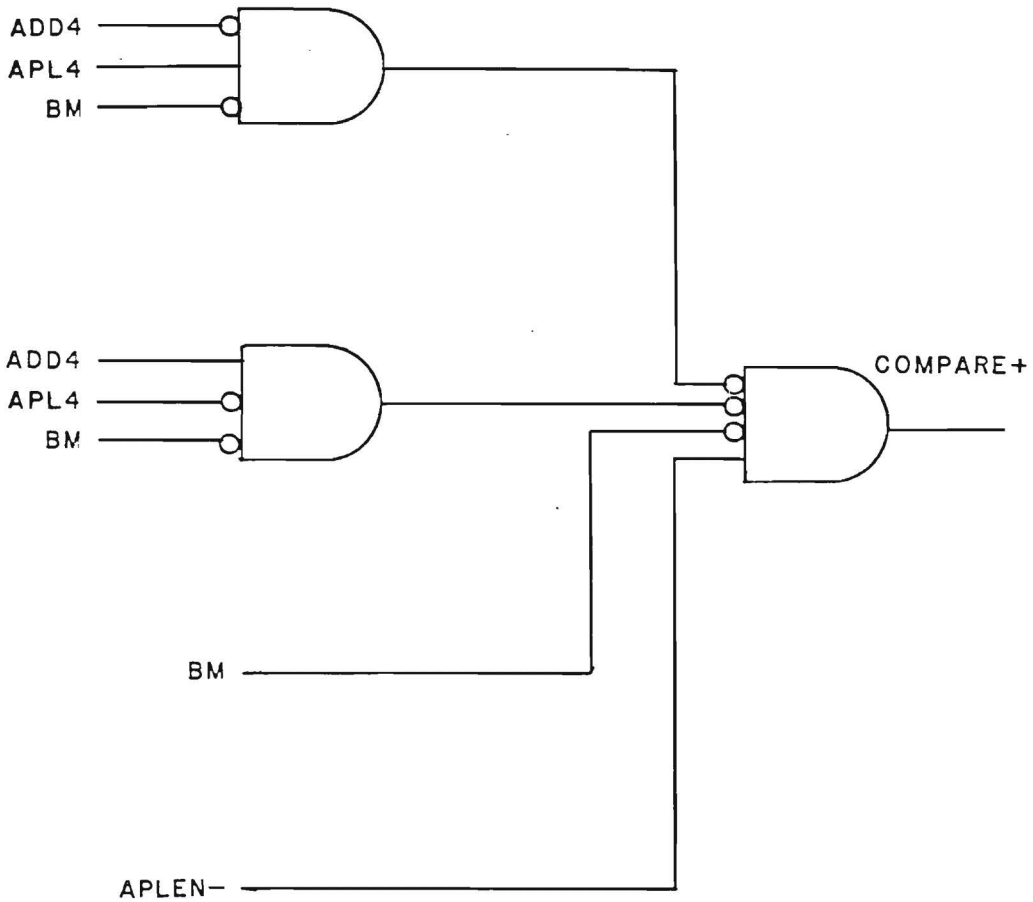


FIGURE 3-10F PAL U9

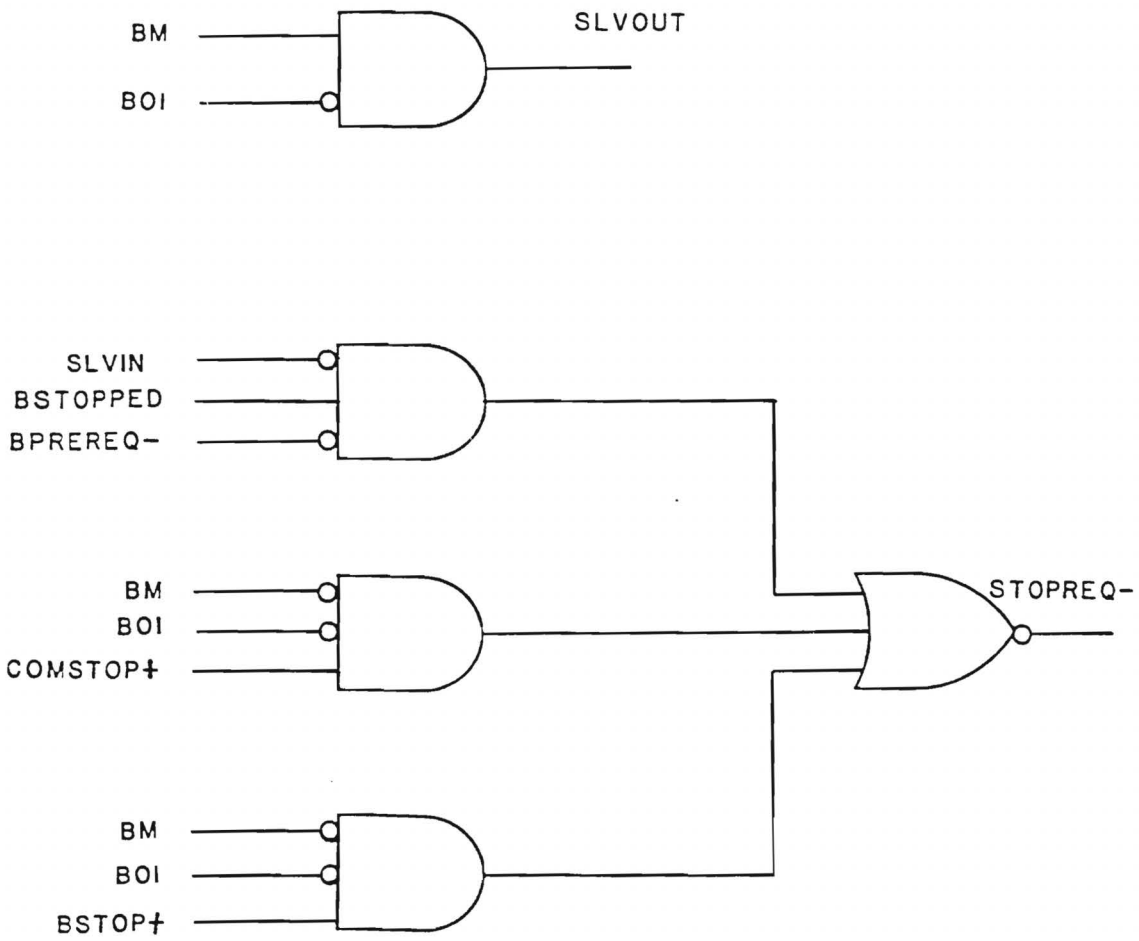


FIGURE 3-11A PAL U7

and direct operand fetches. If the adapter is connected to a master CPU, then SLVIN can generate the stop interrupt. This condition, however, is only intended to cause the Master CPU to perform a console instruction read, so that the Slave CPU can request a cycle on the I/O bus. The PAL only recognizes SLVIN if the Master CPU is not running, and PREREQ is asserted.

Figure 3-11B: PAL U7 controls a run indicator on the Control Panel. PAL U7 signal BRUN is asserted when the adapter U4A signal RUN- indicates that the CPU has halted. The PAL allows one exception to this rule. If the RWR CPU enters a wait state while it is waiting for the I/O bus, the PAL will not assert BRUN.

Figure 3-11C: BADDAT 2, 3, and 4 are gated onto BIB 2, 3, and 4 during a console instruction read.

3.2.6 PAL U28

PAL U28 (Figure 3-12) monitors the DS lines and the Data-In strobe lines to determine when an input device has been selected. DIR will allow U24 and U25 to drive the I/O bus during inputs of these device codes.

This PAL is also used to invert the BSTRBA signal for U31.

3.3 Functional Analysis

This section of the report describes sections of the adapter circuitry that function together. This point of view leads to the description of adapter operations, rather than detailed signal descriptions. When ** appears after a signal name, the numbers replaced by the asterisk are arbitrary. This nomenclature indicates that the function is a signal from a bus. The timing diagrams show typical signal/event propagation, in keeping with the information available on the RWR CPU. Asynchronous input signals are shown as delays from edge to edge, but all signals whose occurrence is timed by the CPU are shown relative to the previous clock edge.

3.3.1 DX Buffer Operation

The DX observes the operation of the RWR CPU through the DX buffer on the adapter (Figure 3-1). During each memory access in the RWR CPU, the DX buffer captures both an address word and a data word for later evaluation by the DX.

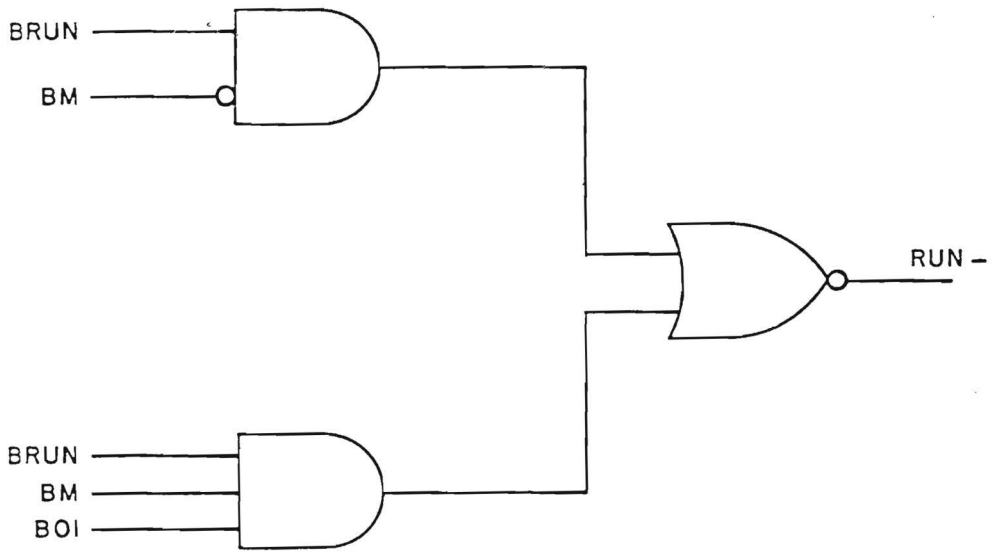


FIGURE 3-11B PAL U7

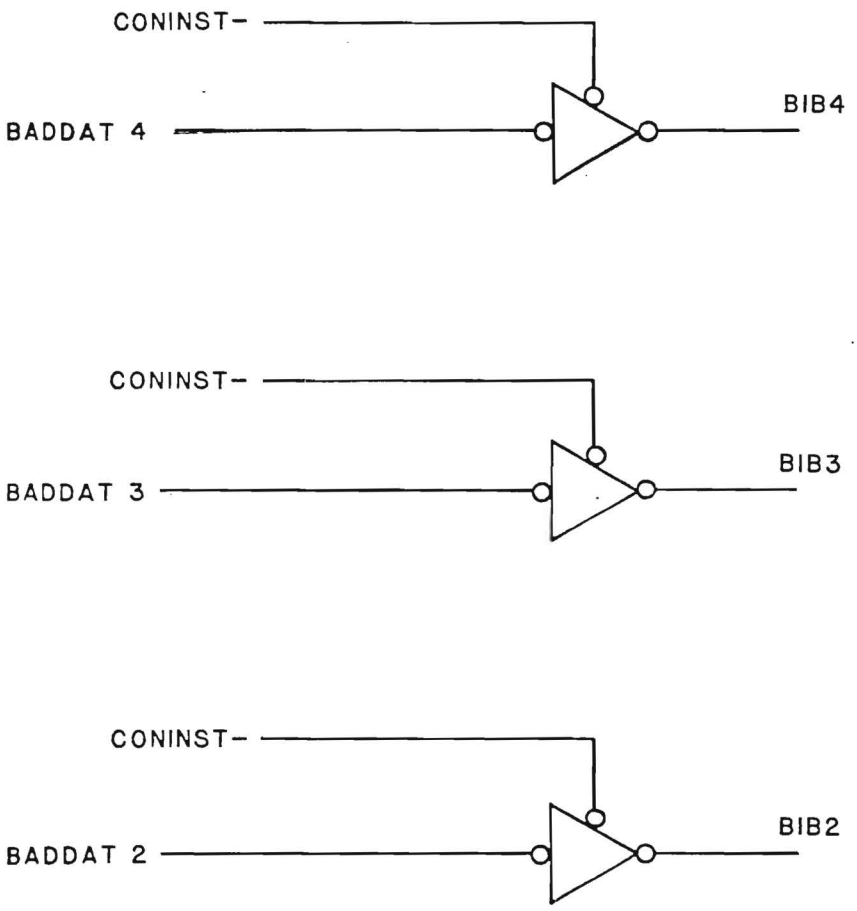


FIGURE 3-11C PAL U7

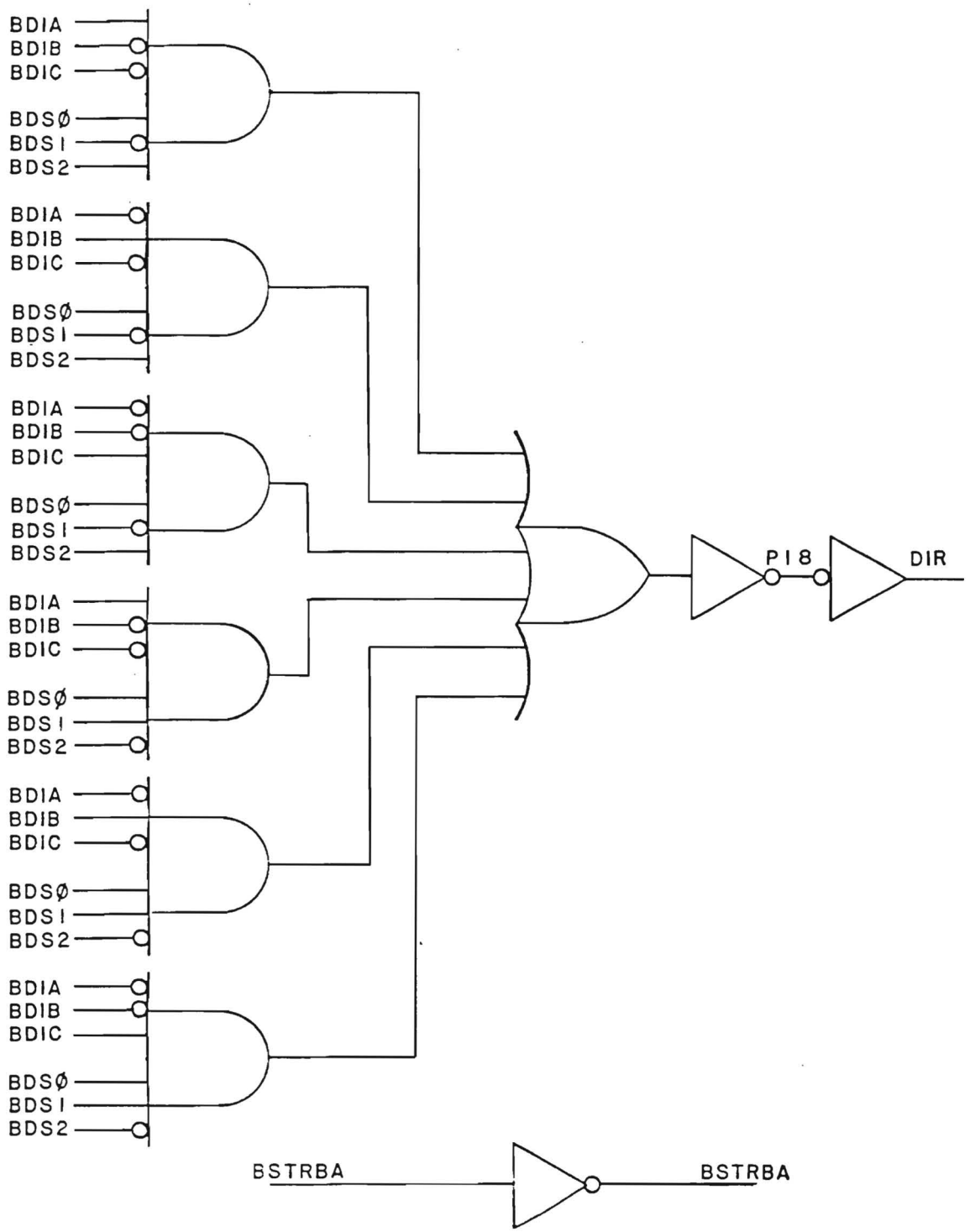


FIGURE 3-12 PAL 28

Figure 3-13: PAL U3 latches the address word into the DX buffer on the trailing edge of the BSTRBA- timing strobe with the signal MADD+. PAL U3 uses FETCH- to clock latch U5B on the trailing edge of BSTRBA- when the cycle is an instruction fetch. This produces DXFETCH+, which is inverted by U8 to produce DXFETCH-. The immediately following leading edge of the timing strobe BSTRBD- clears latch U5B, raising DXFETCH-. This action helps the DX sort out the flow of execution in the RWR CPU. PAL U3 uses DTG- to trigger U4B on the leading edge of the BSTRBD- timing strobe. One-Shot U4B asserts MDATA+ to make the DX buffer data latch transparent, then latches the data by lowering MDATA+ shortly before the trailing edge of the BSTRBD- timing strobe. This accommodation was necessitated by the read timing of the RWR CPU. The two signals DXR-and DXW- distinguish CPU reads and writes for the DX. All three of the signals DXR-, DXW- and DXFETCH- are qualified by the DXEN- signal, which indicates that an EEPROM-CPU is plugged into the RWR. These three signals, as well as the demultiplexed address and data information pass on to the DX.

3.3.2 APL Operation

The automatic program load cycle begins with the CPU in a wait state. The operator at the Control Panel keys the starting address of the adapter APL ROM program into the Control Panel switches. The most significant five switches will determine the 2K block of memory to map the APL ROM into. The remaining switches are an address in the APL ROM which determines the starting location of the program for the RWR CPU. This feature allows several independent programs to be stored in the APL ROM memory. The programs can be individually executed by changing the starting address on the Control Panel switches.

The operator then presses the program load switch on the Control Panel. The following sequence of signals is shown in Figure 3-14A: The Control Panel generates BCONRQ+ through the ISS Buffer, which causes PAL U2 to assert REQCK+. REQCK+ clocks the Console Interrupt-Request Latch, setting BCONREQ- low. BCONREQ- interrupts the CPU through the CPU Buffer. When the CPU honors the interrupt, the CPU reads a console code from the adapter.

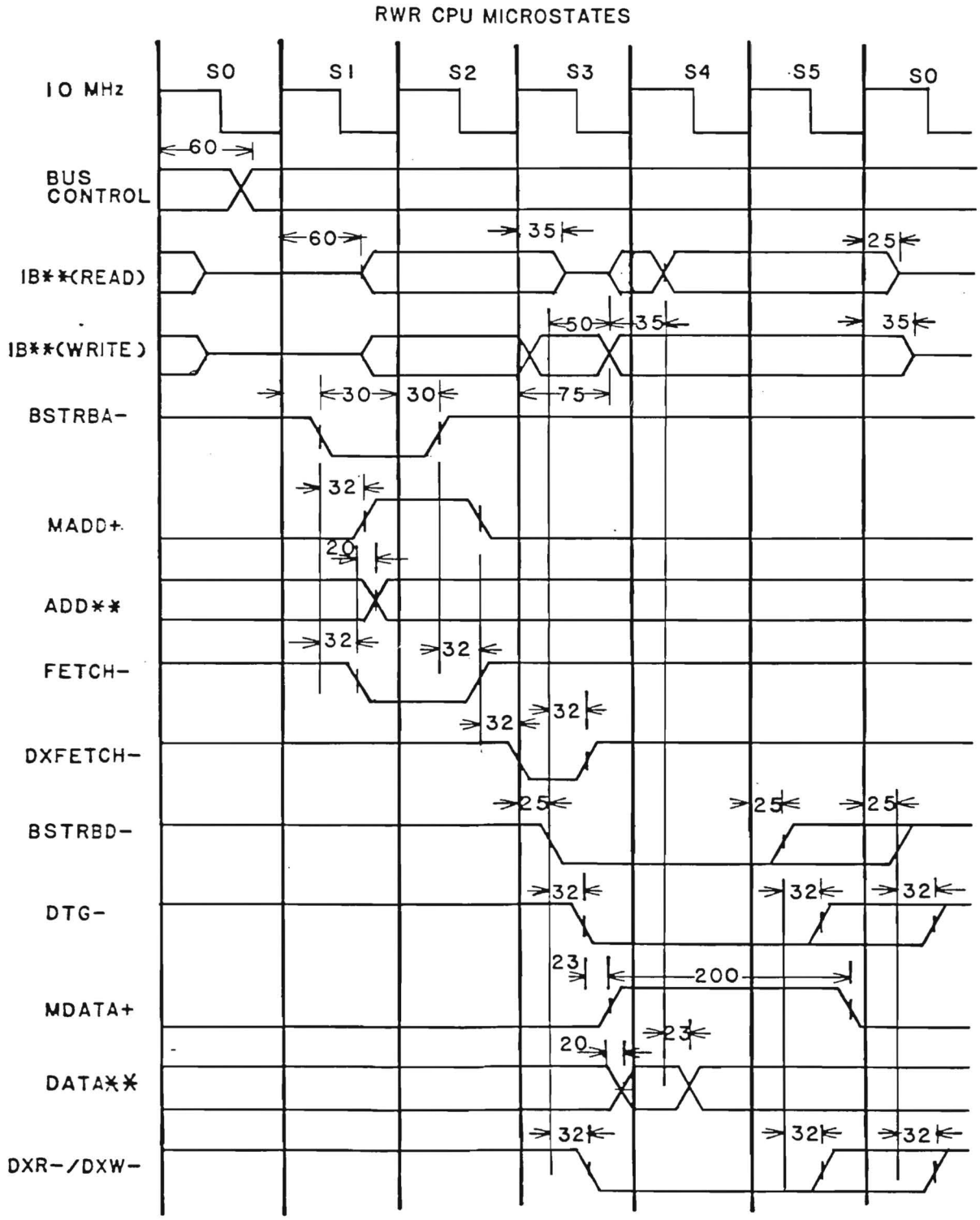


FIGURE 3-13 DX BUFFER TIMING

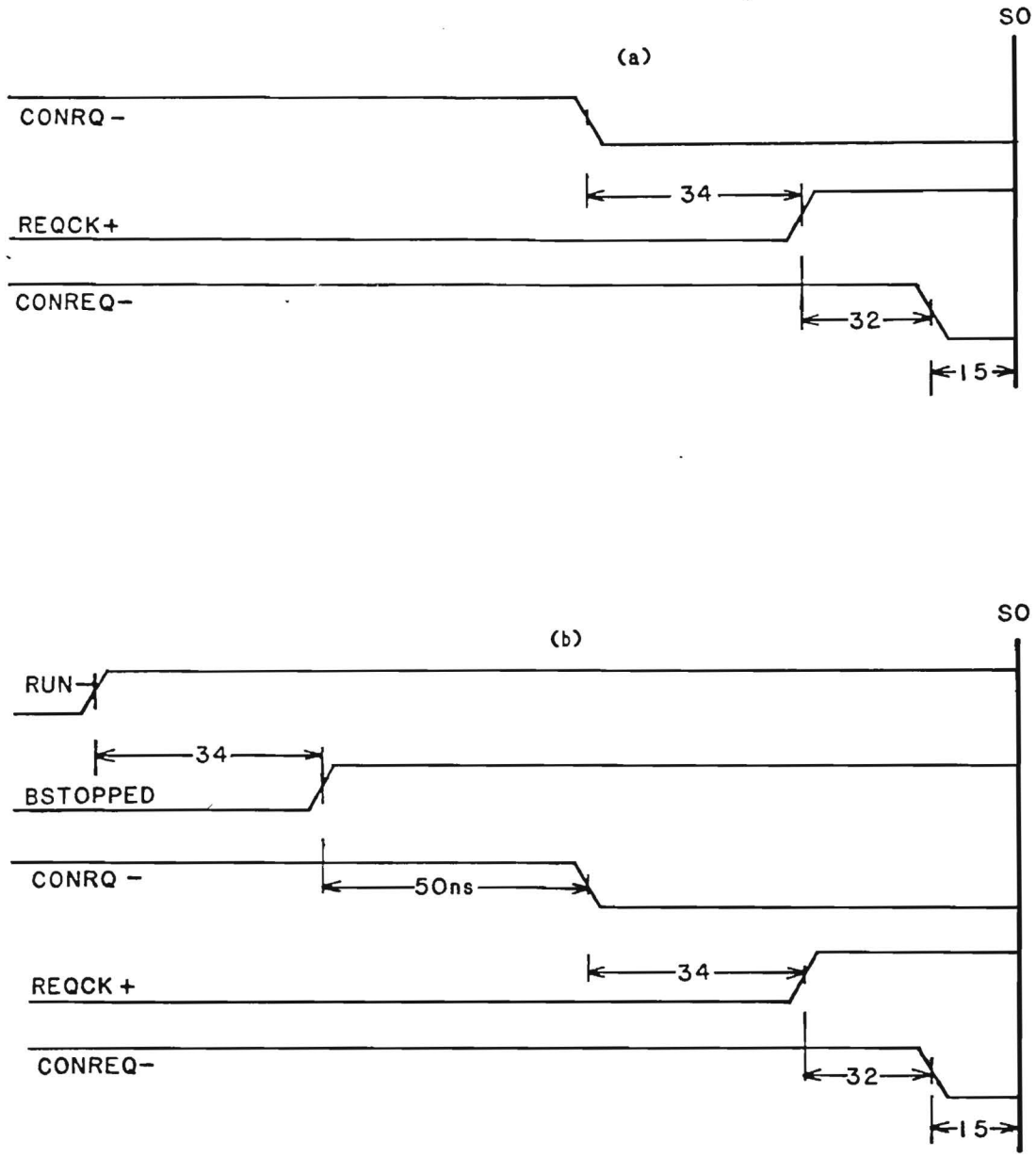


FIGURE 3-14A CONSOLE CODE TIMING

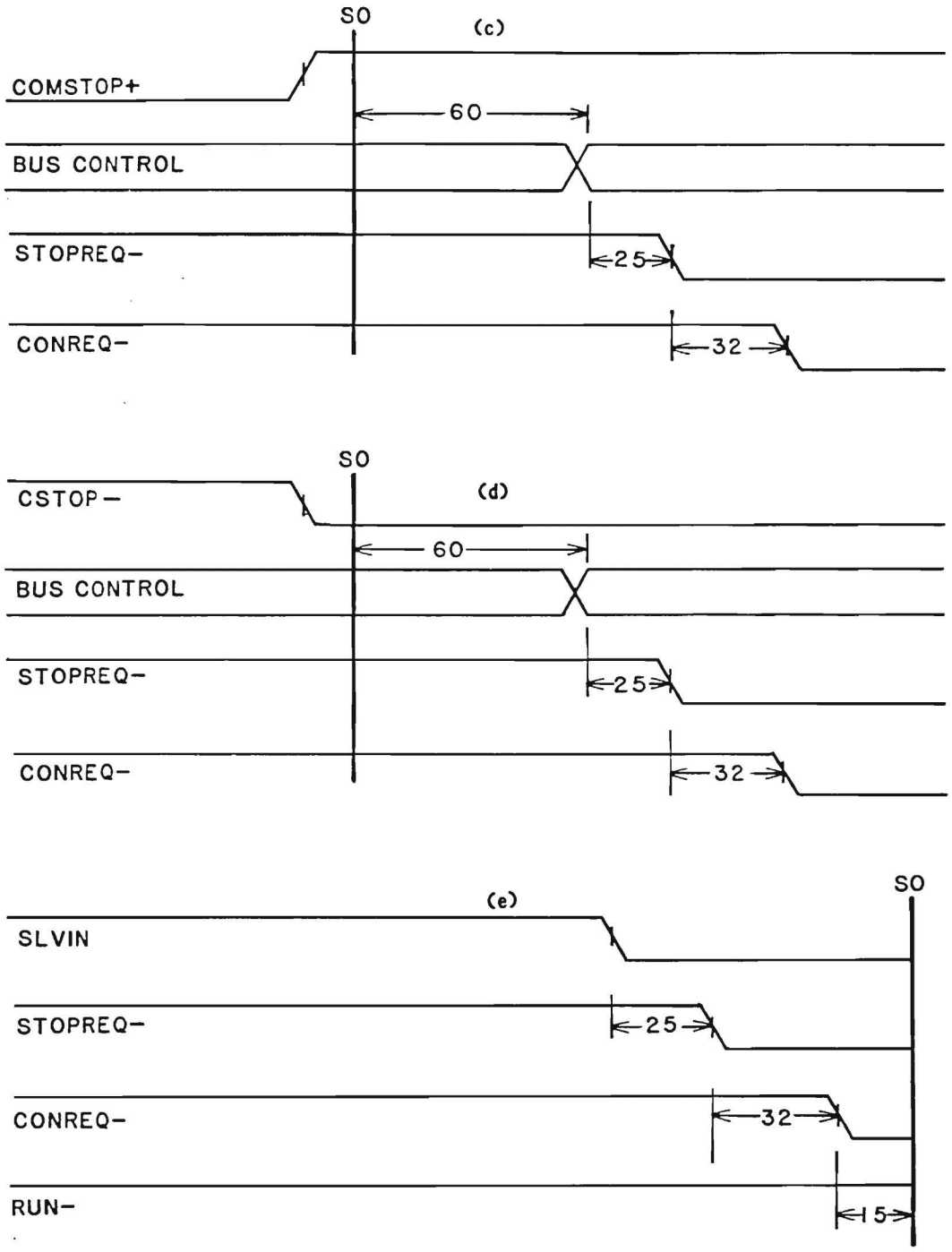


FIGURE 3-14B CONSOLE CODE TIMING

Figure 3-15 shows the timing diagram for the console code read cycle. During this cycle, PAL U2 asserts CONINST-. The leading edge of CONINST- clears the Console Request Latch U5A, raising CONREQ-. CONINST- also causes the Control Panel to drive a console operation code onto the ADDAT bus. The adapter derives the Buffered ADDAT bus from connector J2 through the ADDAT Buffer. The DIR signal generated by PAL U2 is normally high, so that transmission from the buffer is directed onto the adapter Buffered ADDAT bus. This buffer is always enabled, but contentions for the IB are prevented in the Information Interface. Since this cycle is a console code read cycle in the CPU, PAL U3 raises BADDATE-, disabling the Information Interface. PAL U9 translates the code into a CPU START instruction, and drives the machine code onto the Buffered IB. The code is transmitted onto the RWR CPU IB through connector J1 by the adapter IB Buffer. PAL U6 decodes the Control Panel APL operation code and pulls LATCH+ low when the PAL changes state on the trailing edge of BSTRBD-.

The RWR CPU automatically executes a second console cycle. This cycle is depicted in the timing diagram of Figure 3-16. This time the CPU reads the Control Panel switches. PAL U3 asserts BADDATE-, so that U14 and U15 are enabled. The CPU reads the switches through U10 and U11, U14 and U15, and U12 and U13. PAL U2 asserts READS-, which causes the Control Panel to drive the switch settings onto the ADDAT bus. On the trailing edge of the timing strobe BSTRD-, PAL U6 asserts LATCH+, latching the map bits from the Control Panel switches into U20. Clocking U20 also asserts APLEN-, which indicates that a load has occurred since the last adapter reset.

The RWR CPU now resumes normal execution at the address in the Control Panel switches. The unique timing of APL ROM program reads is diagrammed in Figure 3-17. Each instruction fetched by the CPU now comes from the APL ROM program until an instruction is fetched outside the 2K boundary. Since APLEN- is asserted, each time the CPU accesses memory, PAL U9 compares the address latched into the DX Buffer with the most significant bit of U20. If the most significant bits match, PAL U9 asserts COMPARE+. COMPARE+ commands U21 to determine whether a match exists between the other four bits in U20 and the next most significant address bits in the DX Buffer. If the bits all agree, then U21 asserts LOAD+, enabling the APL ROMs; LOAD+ also causes PAL U2 to assert IBREAD-, reversing the direction of

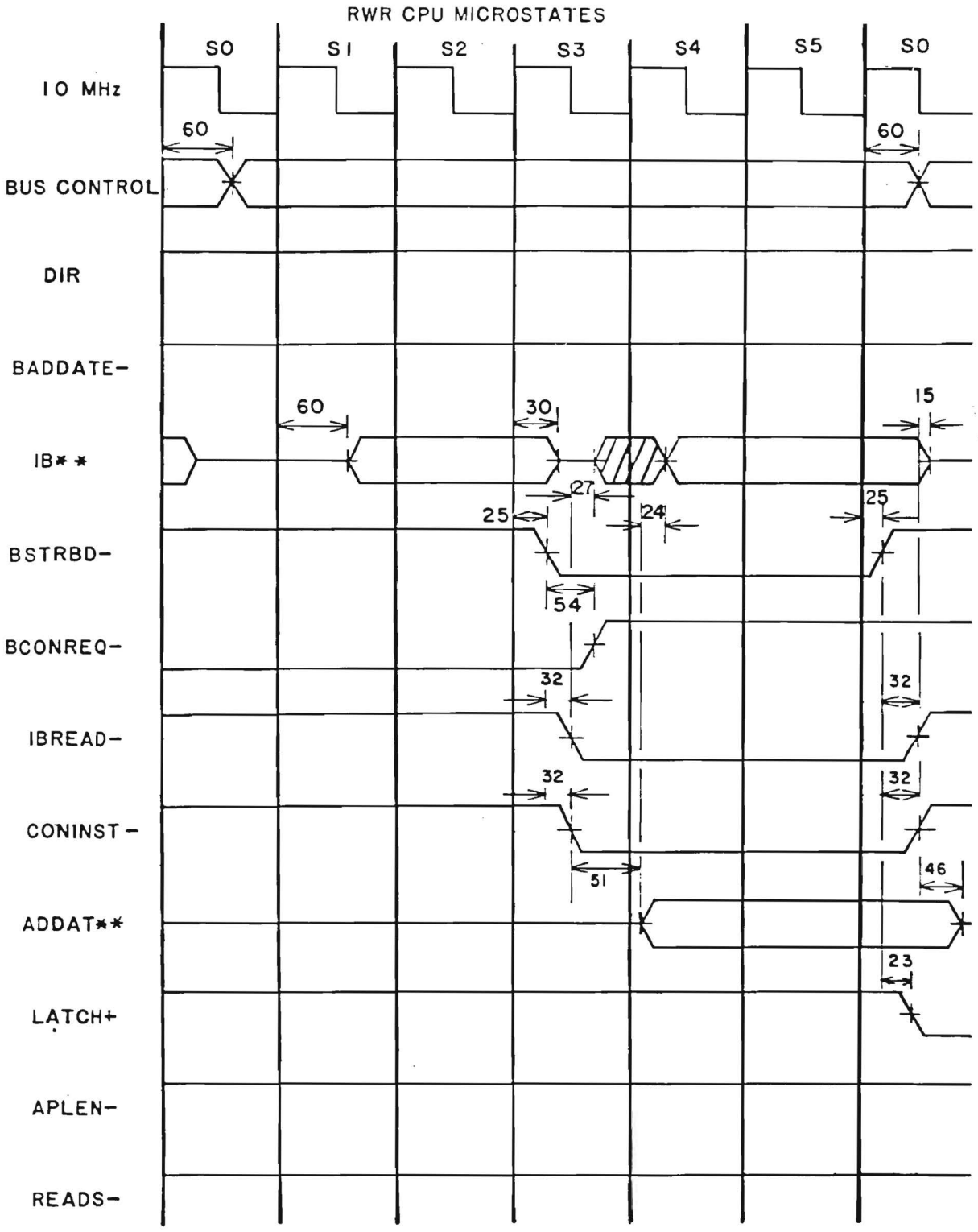


FIGURE 3-15 CONSOLE CODE READ-APL OPERATION

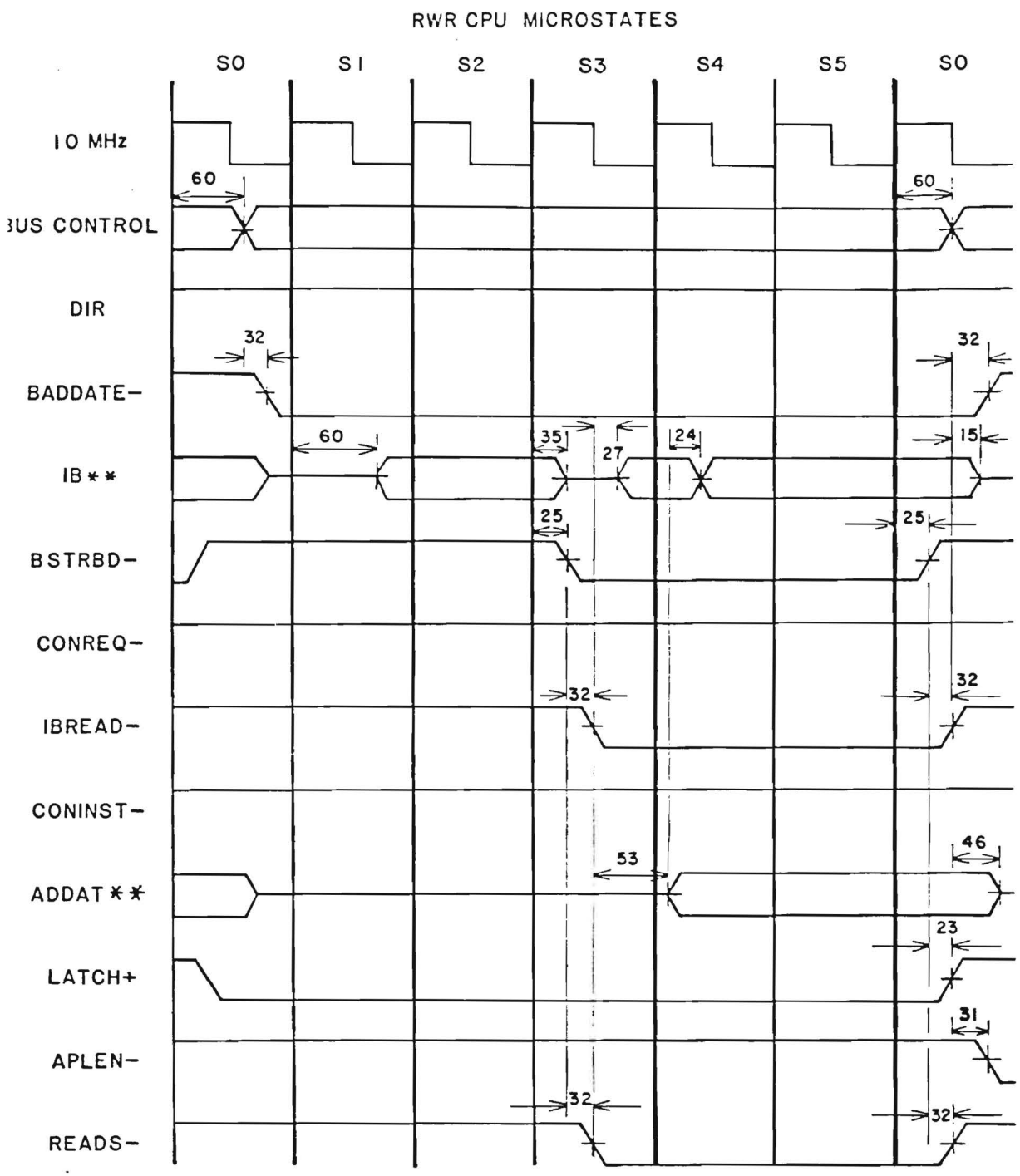


FIGURE 3-16 CONSOLE SWITCH READ

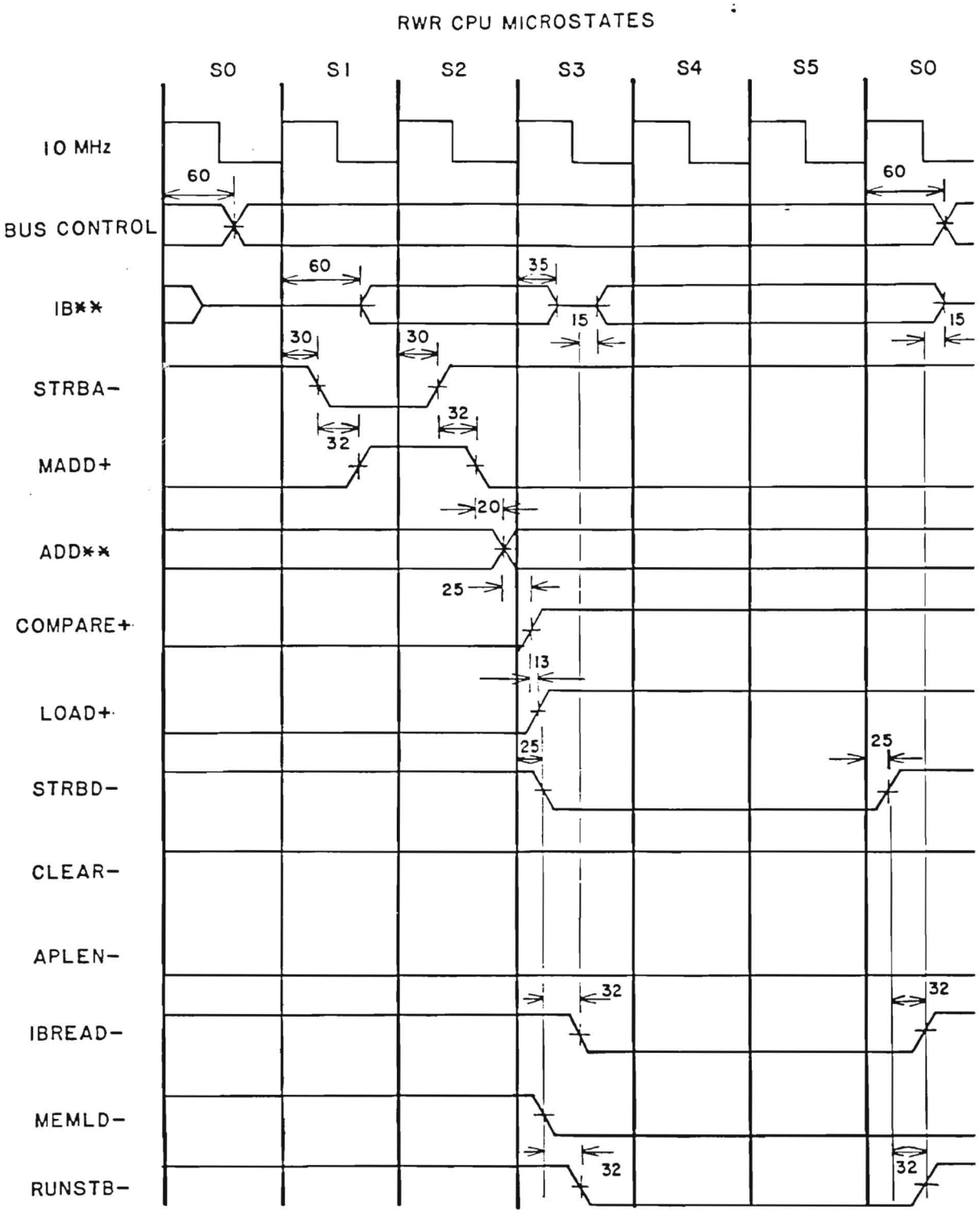


FIGURE 3-17 APL PROGRAM ACCESS

the IB Buffer. LOAD+ further causes PAL U3 to generate MEMLD-, disabling the RWR CPU physical memory. The CPU now reads the data placed on the IB by the APL ROMs.

The adapter will not let the CPU leave the segment of memory occupied by the APL ROMs without removing the APL ROMs from the memory space. This architecture does not assume that the APL ROMs contain all the constants or variables that it might need. In fact, one feature of the architecture is that it does not disturb any locations in the physical memory or the RWR CPU. The program may use this memory, as long as it does not expect to find an instruction outside the 2K block allocated to the APL ROMs. Therefore, no subroutines outside the APL ROMs are allowed. The program in the APL ROMs should contain a HALT or jump to some location outside the program when the program completes. Figure 3-18 shows the first instruction fetch cycle following the completion of the APL ROMs program. When LOAD+ is low, PAL U3 asserts the CLEAR- strobe, which clears U20. This effectively moves the APL ROMs out of the active CPU memory space. CLEAR also raises APLEN-, which disables the APL circuitry until the operator initiates another program load operation. The RWR CPU continues execution normally.

3.3.3 HALT Operation

Console timing is shown in Figure 3-14B(d): When the operator at the Control Panel presses the stop switch, he generates BSTOP+ in U8 of the adapter. BSTOP+ causes PAL U7 to assert STOPREQ-, which clears U5A. Clearing U5A asserts BCONREQ-, interrupting the RWR CPU. There is no further action in the Control Panel, and the code driven onto the ADDAT bus from the Control Panel is the default code. PAL U2 generates the signal CONINST- during the console code read, and PAL U9 drives the halt code onto the IB bus, to be read by the RWR CPU. The COMSTOP+ signal from the DX interface affects the adapter in the same way. Both COMSTOP+ and BSTOP+ are qualified in PAL U7 by the bus control signals that indicate a CPU instruction fetch or direct operand fetch. Figure 3-14B(c) shows the timing for this stop request.

It is possible for the Master CPU to be halted from the Master CPU's Control Panel, so that the Slave CPU can be operated independently. But this creates an unusual situation which cannot exist in the flight software

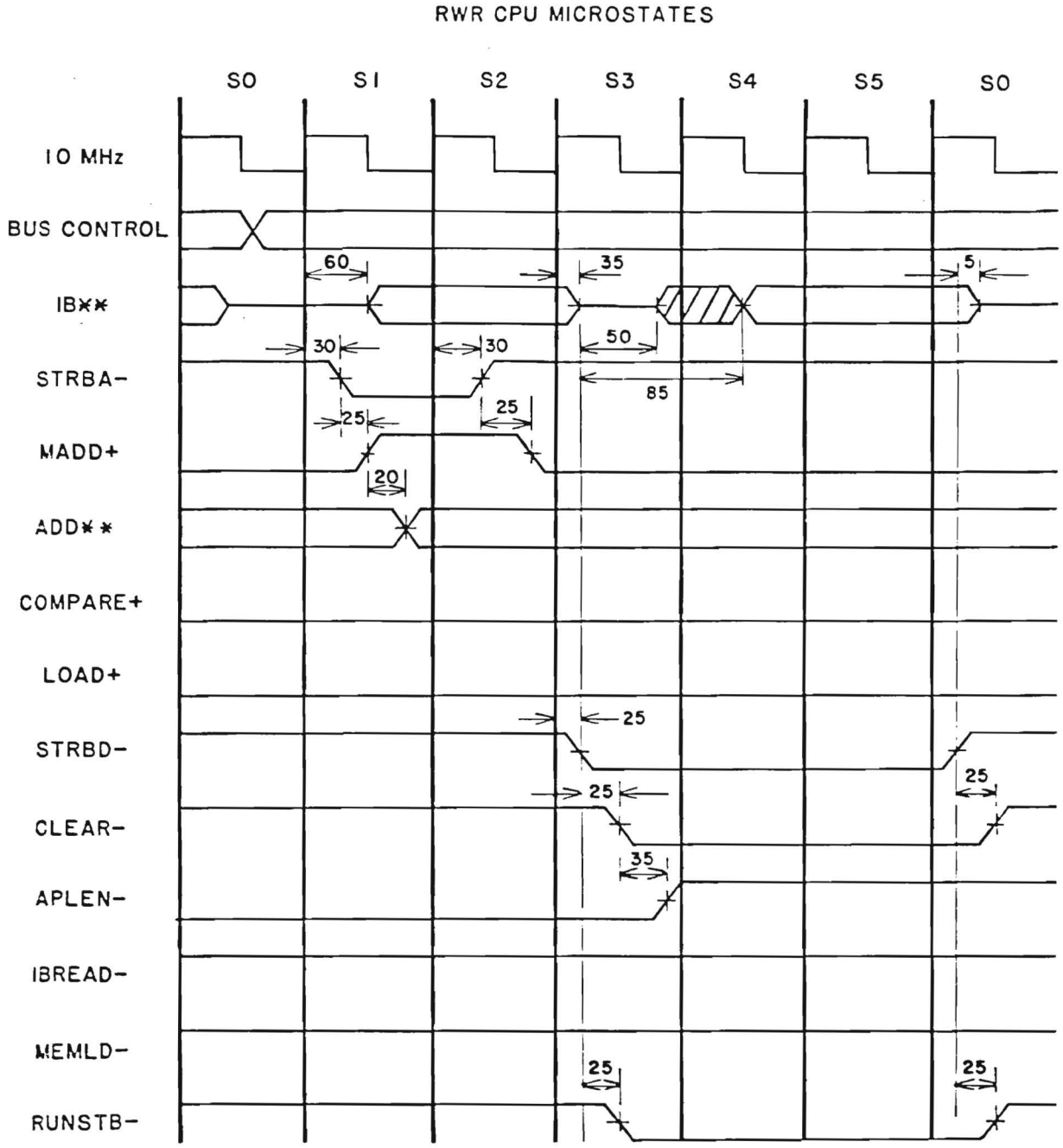


FIGURE 3-18 APL PROGRAM COMPLETION

for the RWR. This test condition creates a status in the RWR that prevents the Slave CPU from being granted the I/O bus. To circumvent this problem, the SLVIN input to the Master CPU's adapter causes the same sequence of operations in the Master CPU that are caused by BSTOP+ and COMSTOP+. Figure 3-14B(e) shows the timing diagram. Although the Master CPU is already halted, it honors the console request (CONREQ-) generated by U5A. The Master CPU performs the console code read but, during the read, it grants the I/O bus to the Slave CPU. The Master CPU harmlessly performs the stop sequence without changing the value of any internal registers, or the state of the Control Panel displays.

All three of the signals COMSTOP+, BSTOP+, and SLVIN cause the RWR CPU to enter the same sequence of instructions. This sequence is programmed by the Control Panel logic, and each instruction in the sequence results in a similar set of adapter operations. The first action to take place happens in the adapter. The one-shot U4A detects that the CPU is in a wait state, and raises RUN-. PAL U7 then observes that the CPU is not waiting for an I/O event, by the status of the bus control lines, and asserts STOPPED-. STOPPED- becomes inverted in U8, which produces BSTOPPED, for use at the Control Panel. BSTOPPED is connected to the Control Panel J2-19, the ISS adapter chassis bus B-48, and the DX J3-35. The timeout of U4A, and the first interrupt produced by the adapter, is shown in Figure 3-14A(b).

BSTOPPED starts the stop sequence of the Control Panel. This sequence updates the Control Panel displays. Each console operation begins by generating BCONRQ+. Then the PAL U2 signal REQCK+ clocks U5A, which asserts BCONREQ-. The CPU honors the console operation by reading the console code. PAL U2 detects the console code read, issuing CONINST-, and raising BADDATE-. BADDATE- high disables U14 and U15. CONSINST clears the console request by setting U5A. CONSINST also causes the Control Panel to drive a console operation code onto the ADDAT bus, which is translated by PAL U9 and read by the RWR CPU.

The console operations follow a predefined sequence that examines registers and memory to update the Control Panel displays. Each operation causes an automatic second cycle in the CPU that writes data to the Control Panel. PAL U2 senses the write operation and lowers the DIR line to direct transmission in U14 and U15 and the ADDAT Buffer toward the Control Panel (see Figure 3-19). PAL U3 enables U14 and U15 by asserting BADDATE-.

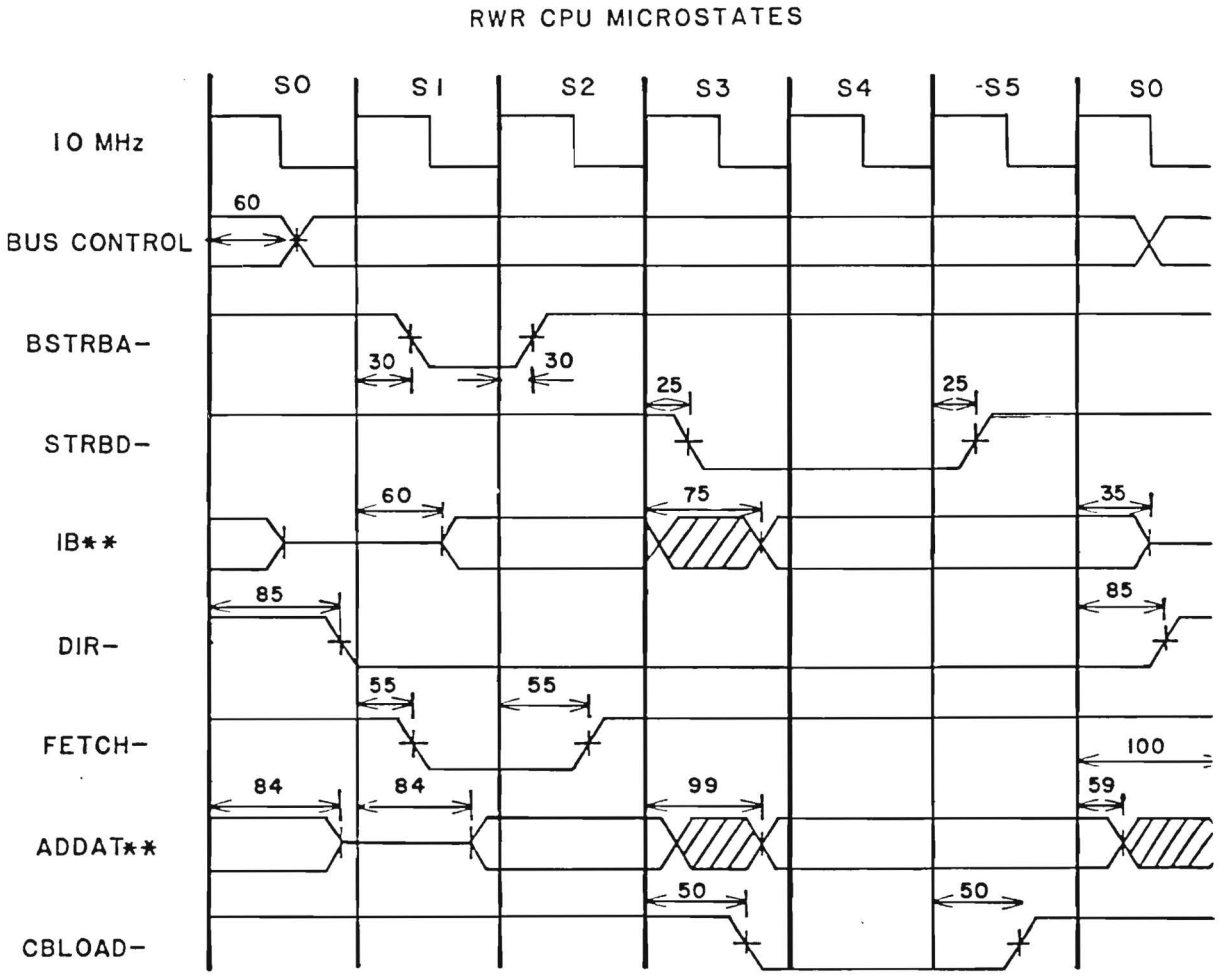


FIGURE 3-19 CONSOLE DATA WRITE

The trailing edge of the CBLOAD- strobe now produced by PAL U2 is steered by the Control Panel circuits to the proper display. CBLOAD- latches the data from the RWR CPU.

3.3.4 Console Operation

If the RWR CPU is already halted, then pressing one of the Control Panel switches causes the execution of the console sequence. The Control Panel generates a console request by generating BCONRQ+ in U8. The CPU reads the console instruction from PAL U9 on the IB, and executes the operation. If the console operation requires two console instructions, PAL U6 generates a second console interrupt request and signals PAL U9 which instruction to place on the IB for the CPU. Figures 3-20, 3-21, and 3-22 show the timing of the two instruction console operations.

If the second cycle of any console instruction requires data to be written to the Control Panel displays, PAL U2 raises DIR- to change the information flow direction of the Information Interface and the ADDAT buffer. PAL U2 asserts CBLOAD- during the BSTRBD timing strobe to enter the data in the Control Panel display. Control Panel logic then steers the data and the strobe to the proper display on the Front Panel.

There are three console operations that require a second instruction from PAL U9. The adapter implements the START instruction by loading an address from the Control Panel switches into the RWR CPU program counter, and then the adapter signals the RWR CPU to continue from that address. The adapter implements the APL auxiliary program load instruction by loading an address into the RWR CPU program counter and continuing. This time, however, the adapter also maps the APL ROM circuits into the RWR CPU memory space. The adapter implements the one-instruction-step operation by signalling the RWR CPU to continue from the current address in its program counter. The adapter then immediately halts the CPU, and signals the Control Panel to begin the display update sequence. The console code-read cycle in which PAL U6 detects the special operation sets SPEC-. DEL- is also set if the operation requires a CONTINUE as the second RWR CPU instruction. The intermediate cycle that follows is either a console switch-read or an instruction fetch. During this cycle, PAL U6 causes PAL U2 to request another console operation. A second console code-read cycle follows. If the CPU is running when one of the Control Panel operation

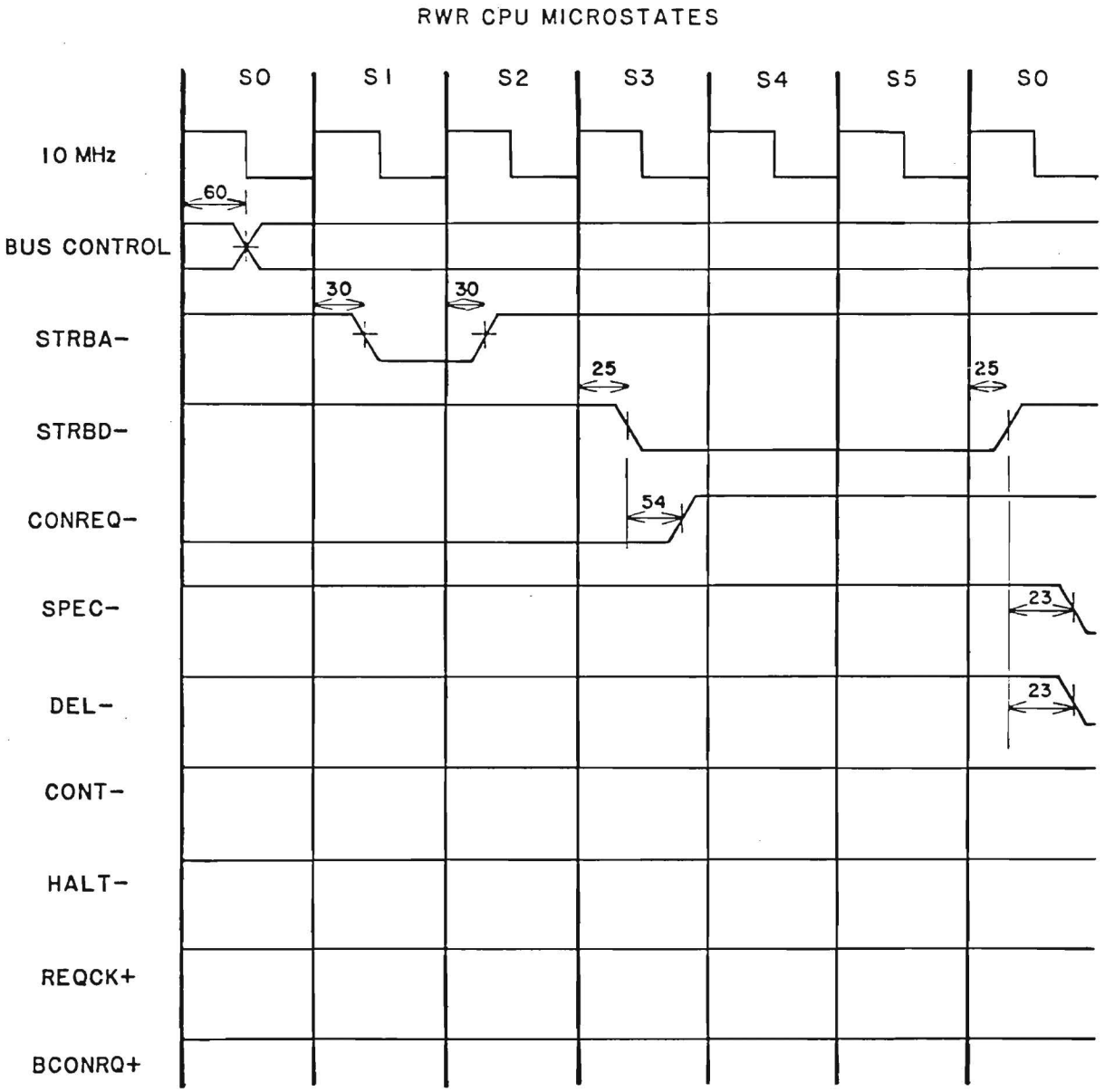


FIGURE 3-20 FIRST CONSOLE CODE READ

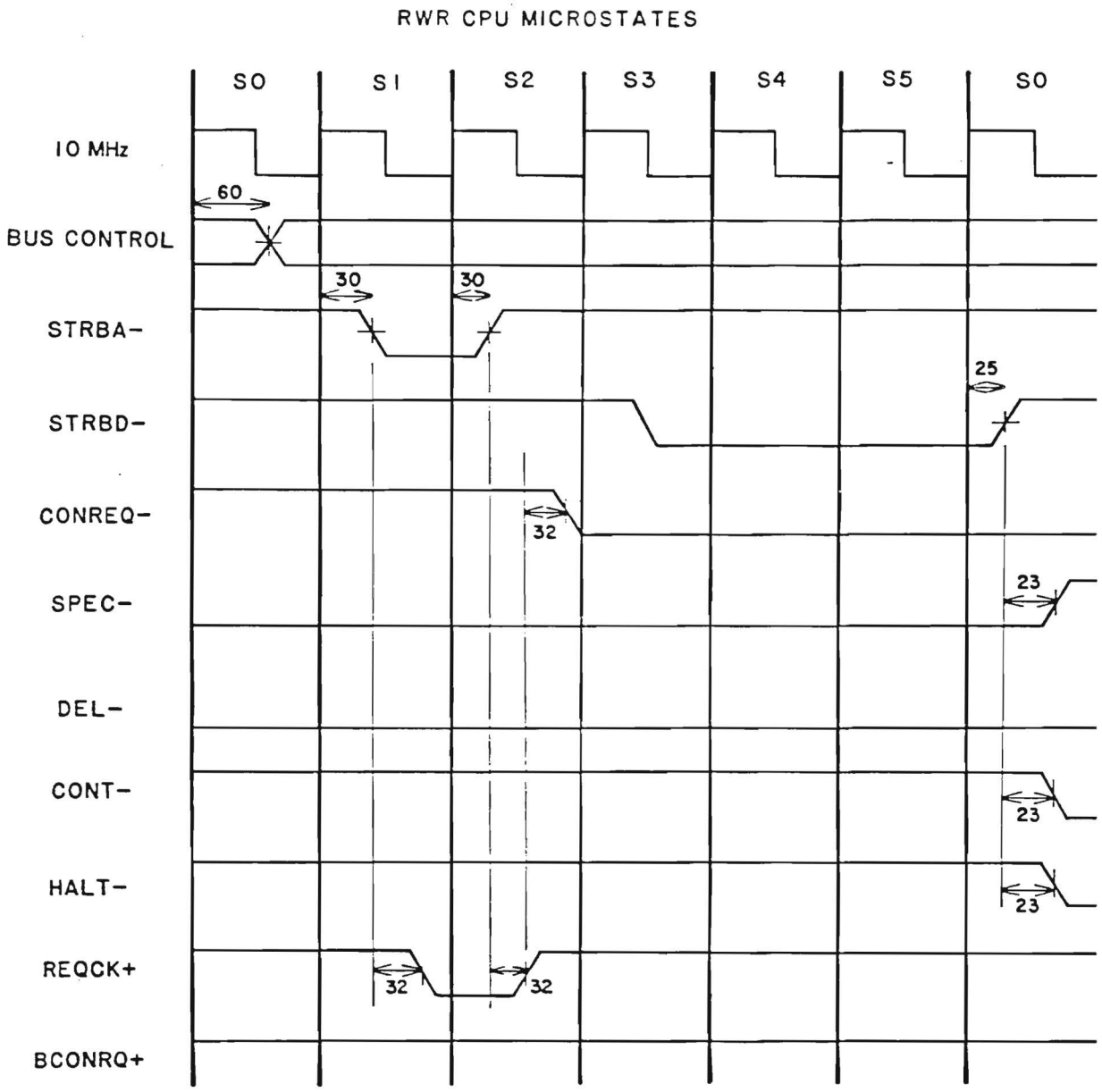


FIGURE 3-21 INTERMEDIATE CYCLE

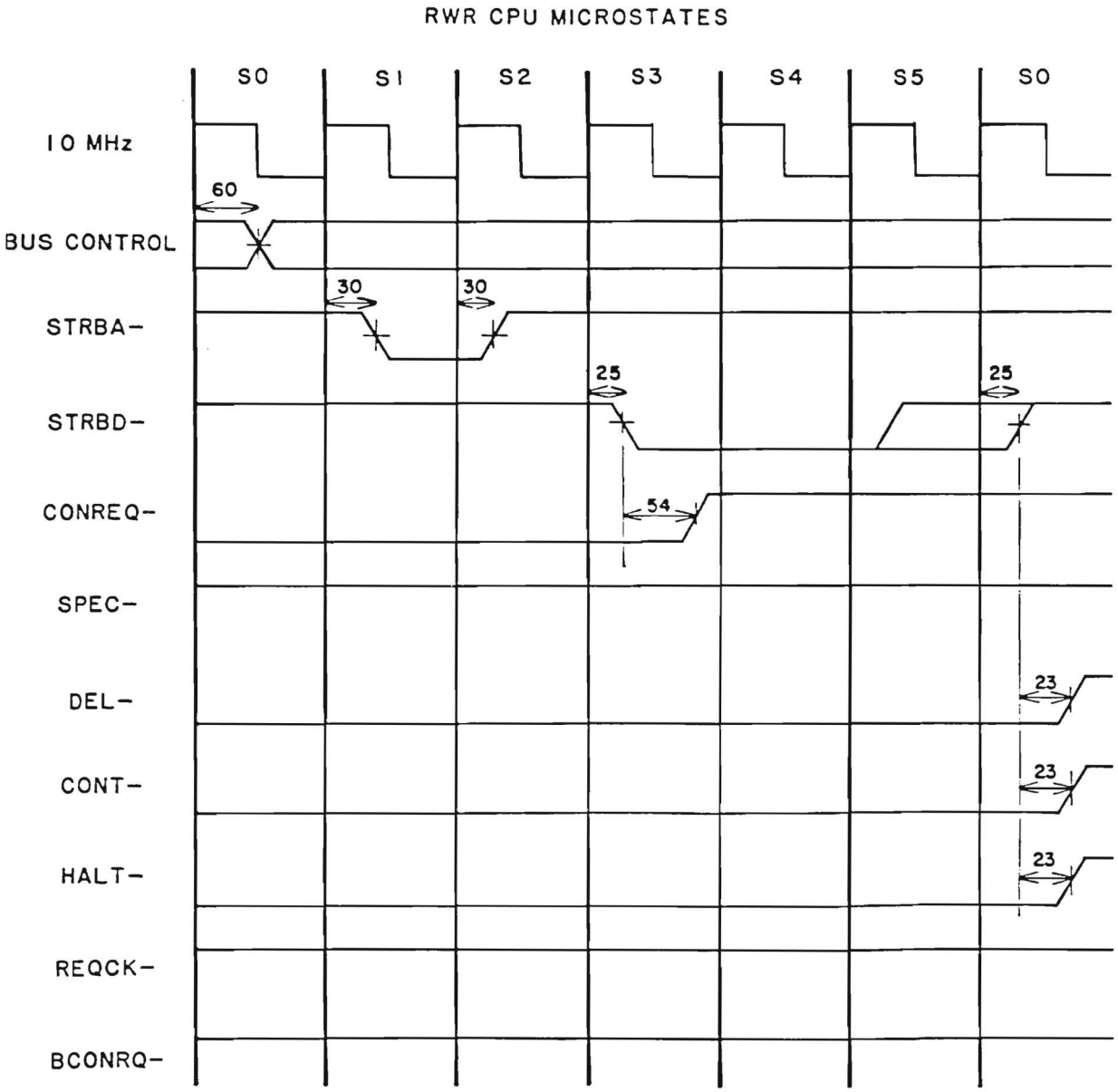


FIGURE 3-22 SECOND CONSOLE CODE READ

switches (other than STOP or RST) is pressed, the CPU will ignore the switch.

3.3.5 Address Window Update

During normal execution in the RWR CPU, the address window on the Control Panel display is kept updated with the address of the current instruction. Each time an instruction is fetched, PAL U2 lowers DIR to change the direction of transmission in U14 and U15 and the ADDAT Buffer toward the Control Panel. The address placed on the information bus by the RWR CPU then passes through the IB Buffer, U14 and U15, and the ADDAT Buffer to the Control Panel. PAL U3 asserts FETCH- during the timing strobe BSTRBA-, and the trailing edge of FETCH- latches the address into the Control Panel address window.

A special condition is provided for the case of the CPU honoring console-request at the end of a direct operand-fetch cycle. In this case, the data in the window on the Control Panel does not correspond to the address in the address window unless the adapter updates the address window with the address of the direct operand. PAL U3 detects that the processor will stop, and updates the address in the same manner described in the last paragraph.

4.0 INSTALLATION

4.1 Jumpers

There are two jumper options selectable on the adapter interface. Both (E1 and E2) are used to allow the slave CPU to access the I/O bus when the master CPU is halted. E1 will be installed on the master adapter board and E2 will be installed on the slave adapter board.

4.2 Potentiometers

There is only one potentiometer (R2) on the adapter board. This potentiometer is used to control one-shot U4B during the strobe data time of memory cycles. To adjust R2, disconnect all adapter cables and ground J1-38. Inject a 1 MHz or less square wave into J1-39 while monitoring J2-29. Adjust R2 until the low going pulse on J2-29 is between 250 ns and 300 ns in duration.

4.3 Master/Slave Installation

When an adapter board is used with a Slave CPU, it is necessary to remove U24, U25, U26, and U27 from the adapter. All I/O signals (except for the DS lines) will be buffered by the Master adapter board. The Slave DS lines will be buffered by U31 on the Slave adapter board when the Slave has control of the I/O bus.

APPENDIX A

PAL LOGIC EQUATIONS

```
PAL16L8
PAT001
A3183 ADAPTER---CONTROL PAL U2
J.T. PARISH

W M 01 00 STRBD LOAD SPEC DXEN BCONRQ GND
STRBA DXR DXW CONINST CBLOAD READS DIR IBREAD REQCK VCC


REQCK = /BCONRQ + /SPEC*/STRBA
IBREAD = W*M*01*/STRBD + LOAD*/STRBD*W
DIR = /W + /M*/01
READS = M*01*00*/STRBD*W
CBLOAD = M*01*00*/STRBD*/W
CONINST = M*01*/00*/STRBD
IF (/DXEN) DXR = W*/M*/STRBD
IF (/DXEN) DXW = /W*/M*/STRBD

DESCRIPTION:

    THIS PAL CONTAINS ALL OF THE DATA STROBES FOR THE ADAPTER AND CONSOLE
CIRCUITRY.  THE PAL ALSO CONTROLS THE DIRECTION OF THE BUFFERS ON THE
ADAPTER.  FINALLY, THE SIGNAL WHICH SETS THE INTERRUPT REQUEST FLIP FLOP
FOR CONSOLE OPERATIONS IS CLOCKED BY THIS PAL.
```

```
PAL16L8
PAT001
A3183 ADAPTER---CONTROL PAL U3
J.T. PARISH

M 01 00 STRBA STRBD W DXEN BCONRQ RESET GND
LOAD RUNSTRB MADD DCH FETCH BADDATE CLEAR DTG MEMLD VCC

DTG                  = /M*/STRBD
CLEAR                = /RESET + /LOAD*/STRBD*/M*/01*/00
IF(/DXEN) FETCH      = /M*/01*/00*/STRBA + /M*/01*00*BCONRQ*/STRBA
DCH                  = M*/01*00
MADD                 = M + STRBA
RUNSTRB              = /M*/01*/00*/STRBD + M*/01*/STRBD
BADDATE              = M*01*00  + /M*/01
IF(W) MEMLD          = LOAD

DESCRIPTION:
    THIS PAL ENABLES THE ADAPTER BUFFERS.  THE PAL ALSO GENERATES
SEVERAL CONTROL STROBES WHICH EXERCISE THE DX INTERFACE AND
SEND INSTRUCTION AND/OR OPERAND ADDRESSES TO THE CONSOLE PANEL.
```

```
PAL16R8
PAT001
A3183 ADAPTER---INSTRUCTION CODE SYNCHRONIZER U6
J.T. PARISH

STRBD I5 I4 I3 I2 CONINST M NC8 NC9 GND
NC11 HALT CONT DEL NC15 NC16 NC17 LATCH SPEC VCC

SPEC    = /I2*/I3*I4*/I5*/CONINST*CONT*HALT + I2*I3*/I4*/CONINST*CONT*HALT
        + /SPEC*M
LATCH   = /CONINST*/I5*I4*/I3*/I2*DEL
DEL     = /I2*/I3*I4*/I5*/CONINST*DEL*CONT*HALT +
          I2*I3*/I4*I5*/CONINST*DEL*CONT*HALT + CONINST*/DEL
CONT    = /SPEC*/DEL*CONT + CONINST*/CONT
HALT    = /SPEC*DEL*HALT + CONINST*/HALT


DESCRIPTION:
     THIS PAL GOVERNS THE OPERATION OF THE MULTIPLE INSTRUCTION
CONSOLE CODE SEQUENCES.  THE PAL THEN CONTROLS THE APL LATCH IN
ACCORDANCE WITH THE TIMING IT ESTABLISHES.  THIS PAL CAN GENERATE CONSOLE
REQUEST CLOCKS THROUGH PAL U2.
```

```
PAL16L8
PAT001
A3183 ADAPTER---MASTER/SLAVE ARBITRATION REGISTER ENCODER U7
J.T. PARISH

M 01 4 3 2 CONINST BSTOP COMSTOP RUN GND
SLAVIN NC12 BIB2 BIB3 BIB4 STOPREQ PREREQ SLVOUT BRUN VCC

SLVOUT       = M*/01
STOPREQ      = /SLAVIN*RUN*/PREREQ + /M*/01*COMSTOP + /M*/01*BSTOP
IF(/CONINST) BIB4  = /4
IF(/CONINST) BIB3  = /3
IF(/CONINST) BIB2  = /2
BRUN      = RUN*/M + RUN*M*01


DESCRIPTION:
    THIS PAL ACTS AS THE REGISTER SELECT BUFFER AND SLAVE REQUEST
GENERATOR. THE SIGNAL BRUN IS ALSO GENERATED IN THIS PAL.
```

```
PAL16L8
PAT001
A3183 ADAPTER---INSTRUCTION ENCODER U9
J.T. PARISH

I5 I4 I3 I2 APL4 ADD4 M CONINST CONT GND
HALT COMPARE APLEN BIB5 BIB6 BIB7 BIB8 BIB9 BIB0 VCC

IF (/CONINST) BIB0 = I3*/I4 + I3*I5 + /I3*I4
IF (/CONINST) BIB5 = /HALT + /CONT + HALT*CONT*I2*I4 + HALT*CONT*I2*/I5
IF (/CONINST) BIB6 = /HALT + HALT*CONT*I5 + HALT*CONT*/I2
IF (/CONINST) BIB7 = /I5 + I3*I4 + I2 + /I3*/I4
IF (/CONINST) BIB8 = /I4*/I5 + /I3*I5
IF (/CONINST) BIB9 = I3*/I4 + I3*I5 + /I3*I4
COMPARE            = /ADD4*APL4*/M + ADD4*/APL4*/M + M + APLEN

DESCRIPTION:
     THIS PAL PRODUCES ALL THE CONSOLE CODES FOR THE 9445.  IN AN AUXILIARY
FUNCTION, THE PAL IDENTIFIES MEMORY CYCLES IN WHICH THE APL COMPARATOR SHOULD
BE ENABLED.
```

```
PAL16L8
PAT001
A3183 I/O BUS BUFFER U28
T.E. TIBBITTS

BDIA BDIB BDIC BDS0 BDS1 BDS2 BDS3 BDS4 BDS5 GND
 BSTRBA BBSTRBA P13 P14 P15 P16 P17 P18 IODIR VCC

IODIR = P18
P18 = BDIA*/BDIB*/BDIC*BDS0*/BDS1*BDS2+/BDIA*BDIB*/BDIC*BDS0*/BDS1*BDS2+
 /BDIA*/BDIB*BDIC*BDS0*/BDS1*BDS2+BDIA*/BDIB*/BDIC*BDS0*BDS1*/BDS2+
 /BDIA*BDIB*/BDIC*BDS0*BDS1*/BDS2+/BDIA*/BDIB*BDIC*BDS0*BDS1*/BDS2
BBSTRBA = BSTRBA



DESCRIPTION:
    THIS PAL SETS THE DIRECTION OF DATA FLOW ON THE I/O BUS AND INVERTS THE
SIGNAL BSTRBA.
```

APPENDIX B

PARTS LIST

DWG: A3183-Ø11-E4

EEPROM/CPU-ISS ADAPTER

Parts List

Item	Quantity	Part Number	Designator	Description
1	7	74LS245	U1, U1Ø, U11, U12, U13, U14, U15	Octal Three-State Transceiver
2	4	PAL16L8	U2, U3, U7, U9	PAL
3	1	74LS123	U4	Dual One-Shot
4	1	74LS74	U5	Dual D-Type Flip-Flop
5	1	74LSØ4	U29	Hex Inverter
6	1	74LS240	U8	Octal Buffer
7	5	74LS373	U16, U17, U18, U19, U31	Octal D-Type Latch
8	1	74LS174	U2Ø	Hex D-Type Flip-Flop
9	1	74LS85	U21	4-Bit Magnitude Comparator
10	2	28S166	U22, U23	2Kx8 PROM
11	1	PAL16R8	U6	Registered PAL
12	4	74LS645-1	U24, U25, U26, U27	Octal Buffer
13	1	74Ø7	U30	Hex Buffer (O.C.H.V.)
14	1	-	C1	1.0 µF Capacitor ±10%
15	1	-	C2	10 pF Capacitor ±10%
16	2	-	C3, C4	20 pF Capacitor ±10%
17	1	-	C5	100 pF Capacitor ±10%
18	1	-	C6	10 µF Capacitor ±10%
19	20	-	C7-C27	0.1 µF Capacitor ±10%
20	1	-	R1	240K ohm Resistor ±5%
21	1	-	R2	20K ohm Resistor (Potentiometer)

Item	Quantity	Part Number	Designator	Description
22	3	-	R3, R4, R8	4.7K ohm Resistor ±5%
23	3	-	R5, R6, R7	1K ohm Resistor ±5%
24	1	-	R9	50 ohm Resistor ±5%
25	1	-	R10	330 ohm Resistor ±5%
26	1	-	R11	470 ohm Resistor ±5%

APPENDIX C
SCHEMATICS

APPLICATION			REVISIONS				
QTY REQD	NEXT ASSY	USED ON	ZONE	SYM	DESCRIPTION	DATE	APPROVED

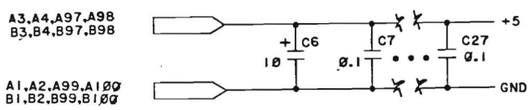
LAST REFERENCE DESIGNATION				
U31	R11	C25		

USED REFERENCE DESIGNATION NOT USED				
NONE	NONE	NONE		

DESCRIPTION		PIN No.	
UNIT No.	I. C. No.	+5V	GND
U1, U10, U11, U12, U13, U14, U15	74LS245	20	10
U2,U3,U7 U9, U28	PAL16L8	20	10
U4	74LS123	16	8
U5	74LS74	14	7
U29	74LS04	14	7
U8	74LS240	20	10
U16, U17, U18, U19	74LS373	20	10
U20	74LS174	16	8
U21	74LS85	16	8
U22, U23	28S166	24	12
U6	PAL16R8	20	10
U24,U25, U26,U27	74LS645-1	20	10
U30	7407	14	7
U31	74LS373	20	10

NOTES: UNLESS OTHERWISE SPECIFIED

1) FOR ALL RESISTORS, VALUES/RATING/ACCURACY ARE OHMS / 1/4W / ±5% RESPECTIVELY
2) FOR ALL CAPACITORS , VALUES/RATING/ACCURACY ARE MICROFARADS/ 10 VOLTS/ ±10% RESPECTIVELY
3) ▽ REPRESENTS A GATE WITH A THREE STATE OUTPUT
4) ⍁ REPRESENTS A GATE WITH OPEN COLLECTOR OUTPUT
5) ⊓ REPRESENTS A GATE WITH SCHMITT-TRIGGER INPUT
6) J1 IS A 50-PIN RIBBON CONNECTOR
7) J2 IS A 40-PIN RIBBON CONNECTOR
8) ALL BUSES ARE LOW TRUE LOGIC



J2-2,J2-33,J2-34,J2-35
J1-4,J1-6,J1-8,J1-10

ITEM OR FIND NO.	QTY REQD		NOMENCLATURE OR DESCRIPTION	MATL SPEC AND SIZE OR COMPONENT VALUE	IDENTIFYING OR PART NO.	CODE IDENT.

PARTS LIST

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMAL ±
FRACTIONS ± ANGLES ± 0°30'
MAX SURFACE ROUGHNESS 125 ALL MACHINED SURFACES EXCEPT AS NOTED
BREAK SHARP EDGES AND CORNERS .010 MAX
FINISH

CONTRACT NO.
DWN TOM COMBES 4 JAN 83
ENGR J. PARISH
CHK [redacted]3
PRO
APV
APVD

EES ENGINEERING EXPERIMENT STATION OF THE GEORGIA INSTITUTE OF TECHNOLOGY ATLANTA, GEORGIA

STANDARD EEPROM CPU ADAPTER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	07101	A3183-011-E4	

SCALE N.T.S. SHEET 1 OF 5

APPLICATION			REVISIONS				
QTY REQD	NEXT ASSY	USED ON	ZONE	SYM	DESCRIPTION	DATE	APPROVED

PROCESSOR CONTROL BUS 2/
DX CONTROL BUS 5/
CONSOLE CONTROL BUS 3/
BUFFER CONTROL BUS 3/
ADAPTER CONTROL BUS 5/
BIB BUS 3/
ADDRESS BUS 1/
BADDAT BUS 4/
TO SHEET 3

PROCESSOR CONTROL BUFFERS
+5V
U1 74LS245
DIR, EN
J1-37 STRBA- 2 A1 B1 18 BSTRBA-
J1-38 M 3 A2 B2 17 BM
J1-39 STRBD- 4 A3 B3 16 BSTRBD-
R10 330Ω, C3 20pF
J1-40 01 5 A4 B4 15 BO1
J1-42 0Ø 6 A5 B5 14 BØØ
J1-43 W- 7 A6 B6 13 BW-
J2-23 RESET 8 A7 B7 12 BRESET-
9 A8 B8 11 CONREQ-
19 EN
J1-32 CONREQ-
J1-45 BRESET-
BCONREQ-
J1-49 MEMLD-

CONTROLLERS
U2 PAL16L8
BW- 1, BM 2, BO1 3, BØØ 4, BSTRBD- 5, LOAD+ 6, SPEC- 7, DXEN- 8, BCONRQ+ 9, BSTRBA- 11
19 REQCK+, 18 IBREAD-, 17 DIR-, 16 READS-, 15 CBLOAD-, 14 CONINST-, 13 DXW-, 12 DXR-

U3 PAL16L8
BM 1, BO1 2, BØØ 3, BSTRBA- 4, BSTRD- 5, BW- 6, DXEN- 7, BCONRQ+ 8, BRESET- 9, LOAD+ 11
19 MEMLD-, 18 DTG-, 17 CLEAR-, 16 BADDATE-, 15 FETCH-, 14 DCH-, 13 MADD+, 12 RUNSTB-

+5V
R1 240K, C1 1.0µF
U4A 74LS123
RUNSTB- 1, +5V 2, 15, 14
1A 1Q 13 NC
1B 1Q 4 RUN-
3
+5V
R2 20K
R3 4.7, C2 10pF
U4B 74LS123
DTG- 9, +5V 10, 7, 6
2A 2Q 5 MDATA+
2B 2Q 12 FETCHD- J2-29
11
+5V
U5B 74LS74
+5V 10, 12
2D 2Q 9 DXFETCH+
FETCH- 11
2CR 2Q 8 NC
13
BSTRBD-

+5V
R4 4.7K
J1-2 DXEN-
EEPROM- J2-28

R5 1K, R6 1K, R7 1K
J1-44 OE-
J1-46 MDREN-
J1-48 WRITE-

INSTRUCTION CODE SYNCHRONIZER
U6 PAL16R8
BSTRBD- 1 CK, BADD 15 2, BADD 14 3, BADD 13 4, BADD 12 5, CONINST- 6, BM 7, NC 8, NC 9, 11 OE
19 SPEC-, 18 LATCH+, 17 NC, 16 NC, 15 NC, 14 DEL NC, 13 CONT-, 12 HALT-

MASTER/SLAVE ARBITER REGISTER ENCODER
U7 PAL16L8
BM 1, BO1 2, BADD 4 3, BADD 3 4, BADD 2 5, CONINST- 6, BSTOP + 7, J3-39 COMSTOP+ 8, RUN- 9
SLAVE 18 E2 SLVOUT B-27
16 STOPREQ-, 15 BIB 4, 14 BIB 3, 13 BIB 2, 12 NC
+5V 4.7K R8
MASTER SLVN 11, B-27 E1, BPRERQ- 17
19 BRUN
DCH- J2-20
READS- J2-21
CONINST- J2-26
CBLOAD- J2-27
FETCH- J2-36

INSTRUCTION CODERS
U9 PAL16L8
BADD 15 1, BADD 14 2, BADD 13 3, BADD 12 4, APL 4 5, ADD 4 6, BM 7, CONINST- 8, CONT- 9, HALT- 11, APLEN- 13
19 BIB Ø, 18 BIB 9, 17 BIB 8, 16 BIB 7, 15 BIB 6, 14 BIB 5, 12 COMPARE+

CONSOLE CONTROL BUFFER
U8 74LS240
J2-24 CSTOP- 2, J2-25 500Ω CONRQ- 4, R9, C4 20pF
A1 Y1 18 BSTOP+
A2 Y2 16 BCONRQ+
14 BPRERQ-
J2-37 PRERQ 6, B-38 BRQENB 8, J1-28 ION 11, J1-26 CARRY 13, BRUN 15, DXFETCH+ 17, DXEN- 19
A3 Y3, A4 Y4 MASTER E3, A5 Y5 9 ION-, A6 Y6 7 CARRY-, A7 Y7 5 BSTOPPED, A8 Y8 3
RQE NB J2-22, B-41, J2-18, J2-17, J2-19, B-48, J3-35
EN 19, EN 1
DXFETCH-

CONSOLE REQUEST LATCH
CONINST-
U5A 74LS74
2 1D 1Q 5 BCONREQ-
REQCK+ 3 CK 1Q 6 NC
1CR 1
STOPREQ-

ITEM OR FIND NO.	QTY REQD		NOMENCLATURE OR DESCRIPTION	MATL SPEC AND SIZE OR COMPONENT VALUE	IDENTIFYING OR PART NO.	CODE IDENT.

PARTS LIST

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMAL ±
FRACTIONS ± ANGLES ± 0°30'
MAX SURFACE ROUGHNESS 125
ALL MACHINED SURFACES EXCEPT AS NOTED
BREAK SHARP EDGES AND CORNERS .010 MAX
FINISH

CONTRACT NO.
DWN TOM COMBES 4 JAN 83
ENGR J. PARISH
CHK [redacted] 2/1/83
PROD
APVD
APVD

GTRI EES ENGINEERING EXPERIMENT STATION OF THE GEORGIA INSTITUTE OF TECHNOLOGY ATLANTA GEORGIA

SCHEMATIC DIAGRAM EEPROM CPU ADAPTER CONTROL CIRCUITS

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	07101	A3183-011-E4	

SCALE N.T.S. SHEET 2 OF 5

APPLICATION			REVISIONS				
QTY REQD	NEXT ASSY	USED ON	ZONE	SYM	DESCRIPTION	DATE	APPROVED

FROM SHEET 2

2 PROCESSOR CONTROL BUS
4 DX CONTROL BUS
3 CONSOLE CONTROL BUS
4 BUFFER CONTROL BUS
6 ADAPTER CONTROL BUS
16 BIB BUS
1 ADDRESS BUS
4 BADDAT BUS

TO SHEET 4

2 2 3 5 16 16 16 16

CONSOLE BUFFER — U10 (74LS245)

DIR−	1	DIR		
J2-16	ADDAT 15	2	A1 B1	18 BADDAT15
J2-15	ADDAT 14	3	A2 B2	17 BADDAT14
J2-14	ADDAT 13	4	A3 B3	16 BADDAT13
J2-13	ADDAT 12	5	A4 B4	15 BADDAT12
J2-12	ADDAT 11	6	A5 B5	14 BADDAT11
J2-11	ADDAT 10	7	A6 B6	13 BADDAT10
J2-10	ADDAT 9	8	A7 B7	12 BADDAT9
J2-9	ADDAT 8	9	A8 B8	11 BADDAT8
		19		

CONSOLE BUFFER — U11 (74LS245)

DIR−	1	DIR		
J2-8	ADDAT 7	2	OE	
J2-7	ADDAT 6	3	A1 B1	18 BADDAT7
J2-6	ADDAT 5	4	A2 B2	17 BADDAT6
J2-5	ADDAT 4	5	A3 B3	16 BADDAT5
J2-4	ADDAT 3	6	A4 B4	15 BADDAT4
J2-3	ADDAT 2	7	A5 B5	14 BADDAT3
J2-2	ADDAT 1	8	A6 B6	13 BADDAT2
J2-1	ADDAT Ø	9	A7 B7	12 BADDAT1
		19	A8 B8	11 BADDATØ

PROCESSOR BUFFER — U12 (74LS245)

IBREAD−	1	DIR		
J1-31	IB15	2	A1 B1	18 BIB 15
J1-29	IB14	3	A2 B2	17 BIB 14
J1-27	IB13	4	A3 B3	16 BIB 13
J1-25	IB12	5	A4 B4	15 BIB 12
J1-23	IB11	6	A5 B5	14 BIB 11
J1-21	IBIØ	7	A6 B6	13 BIB 10
J1-19	IB9	8	A7 B7	12 BIB 9
J1-17	IB8	9	A8 B8	11 BIB 8
		19	OE	

PROCESSOR BUFFER — U13 (74LS245)

IBREAD−	1	DIR		
J1-15	IB7	2	A1 B1	18 BIB 7
J1-13	IB6	3	A2 B2	17 BIB 6
J1-11	IB5	4	A3 B3	16 BIB 5
J1-9	IB4	5	A4 B4	15 BIB 4
J1-7	IB3	6	A5 B5	14 BIB 3
J1-5	IB2	7	A6 B6	13 BIB 2
J1-3	IB1	8	A7 B7	12 BIB 1
J1-1	IBØ	9	A8 B8	11 BIB Ø
		19	OE	

INTERFACE — U14 (74LS245)

DIR−	1	DIR		
BADDATE−	19	OE		
BADDAT 15	2	A1 B1	18	BIB15
BADDAT 14	3	A2 B2	17	BIB14
BADDAT 13	4	A3 B3	16	BIB13
BADDAT 12	5	A4 B4	15	BIB12
BADDAT 11	6	A5 B5	14	BIB11
BADDAT 10	7	A6 B6	13	BIBIØ
BADDAT 9	8	A7 B7	12	BIB9
BADDAT 8	9	A8 B8	11	BIB8

INTERFACE — U15 (74LS245)

DIR−	1	DIR		
BADDATE−	19	OE		
BADDAT 7	2	A1 B1	18	BIB7
BADDAT 6	3	A2 B2	17	BIB6
BADDAT 5	4	A3 B3	16	BIB5
BADDAT 4	5	A4 B4	15	BIB4
BADDAT 3	6	A5 B5	14	BIB3
BADDAT 2	7	A6 B6	13	BIB2
BADDAT 1	8	A7 B7	12	BIB1
BADDATØ	9	A8 B8	11	BIBØ

ADDRESS REGISTERS — U16 (74LS533)

MADD+	11	G		
BIB15	3	ID	1Q	2 ADD15+
BIB14	4	2D	2Q	5 ADD14+
BIB13	7	3D	3Q	6 ADD13+
BIB12	8	4D	4Q	9 ADD12+
BIB11	13	5D	5Q	12 ADD11+
BIB10	14	6D	6Q	15 ADD10+
BIB9	17	7D	7Q	16 ADD9 +
BIB8	18	8D	8Q	19 ADD8 +
DXEN−	1	OE		

ADDRESS REGISTERS — U17 (74LS533)

MADD+	11	G		
BIB7	3	ID	1Q	2 ADD7 +
BIB6	4	2D	2Q	5 ADD6 +
BIB5	7	3D	3Q	6 ADD5 +
BIB4	8	4D	4Q	9 ADD4 +
BIB3	13	5D	5Q	12 ADD3 +
BIB2	14	6D	6Q	15 ADD2 +
BIB1	17	7D	7Q	16 ADD1 +
BIBØ	18	8D	8Q	19 ADDØ +
DXEN−	1	OE		

DATA REGISTERS — U18 (74LS533)

MDATA+	11	G		
BIB15	3	ID	1Q	2 DATA15+
BIB14	4	2D	2Q	5 DATA14+
BIB13	7	3D	3Q	6 DATA13+
BIB12	8	4D	4Q	9 DATA12+
BIB11	13	5D	5Q	12 DATA11+
BIB10	14	6D	6Q	15 DATA10+
BIB9	17	7D	7Q	16 DATA9 +
BIB8	18	8D	8Q	19 DATA8 +
DXEN−	1	OE		

DATA REGISTERS — U19 (74LS533)

MDATA+	11	G		
BIB7	3	ID	1Q	2 DATA7 +
BIB6	4	2D	2Q	5 DATA6 +
BIB5	7	3D	3Q	6 DATA5 +
BIB4	8	4D	4Q	9 DATA4 +
BIB3	13	5D	5Q	12 DATA3 +
BIB2	14	6D	6Q	15 DATA2 +
BIB1	17	7D	7Q	16 DATA1 +
BIBØ	18	8D	8Q	19 DATAØ +
DXEN−	1	OE		

ITEM OR FIND NO.	QTY REQD	NOMENCLATURE OR DESCRIPTION	MATL SPEC AND SIZE OR COMPONENT VALUE	IDENTIFYING OR PART NO.	CODE IDENT.

PARTS LIST

UNLESS OTHERWISE SPECIFIED: ALL CAPACITORS ARE IN MICROFARADS AND ALL RESISTORS ARE IN OHMS, ±5% AND 1/4 WATT.

LAST REFERENCE DESIGNATION USED

U19

INTERPRET THIS DRAWING PER GTEES SPECIFICATIONS AND STANDARDS MANUAL

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMAL ±
FRACTIONS ± ANGLES ± 0° 30'
MAX SURFACE ROUGHNESS 125
ALL MACHINED SURFACES EXCEPT AS NOTED
BREAK SHARP EDGES AND CORNERS .010 MAX
FINISH

CONTRACT NO.

DWN	TOM COMBES	16DEC82
ENGR	J. PARISH	
CHK	[redacted]	12/13
PROD		
APVD		
APVD		

ENGINEERING EXPERIMENT STATION OF THE GEORGIA INSTITUTE OF TECHNOLOGY ATLANTA GEORGIA

SCHEMATIC DIAGRAM EEPROM CPU ADAPTER BUFFER CIRCUITRY

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	07101	A3183-011-E4	

SCALE N.T.S. SHEET 3 OF 5

APPLICATION			REVISIONS				
QTY REQD	NEXT ASSY	USED ON	ZONE	SYM	DESCRIPTION	DATE	APPROVED

FROM SHEET 3

- 2/ PROCESSOR CONTROL BUS
- 2/ DX CONTROL BUS
- 3/ CONSOLE CONTROL BUS
- 5/ ADAPTER CONTROL BUS
- 16/ BIB BUS
- 16/ ADDRESS BUS
- 16/ DATA BUS
- 16/ BADDAT BUS

APL MAPPING LATCH

U20 74LS174 CR

LATCH+ 9 → CK
BADDAT 4 3 → 1D, 1Q 2 → APL 4 1 → 2
BADDAT 3 4 → 2D, 2Q 5 → APL 3 3 → 4
BADDAT 2 6 → 3D, 3Q 7 → APL 2 5 → 6
BADDAT 1 11 → 4D, 4Q 10 → APL 1 9 → 8
BADDAT Ø 13 → 5D, 5Q 12 → APL Ø 11 → 10
+5V → 14 6D, 15 6Q → 13 → 12
CLEAR–
APLEN–

U29 74LS04

APL ADDRESS COMPARATOR

U21 74LS85

ADD 3 15 → A3
ADD 2 13 → A2
ADD 1 12 → A1
ADD Ø 10 → AØ
4 A>B → A>B 5 → NC
2 A<B → A<B 7 → NC
COMPARE+ 3 → A=B → A=B 6 → LOAD+
APL 3 1 → B3
APL 2 14 → B2
APL 1 11 → B1
APL Ø 9 → BØ

APL PROGRAM ROM

U22 28S166

LOAD+ 18 → G3, 19 → G2
BSTRBD– 20 → GT

ADD 5	21	A1Ø	D7 17	BIB Ø
ADD 6	22	A9	D6 16	BIB 1
ADD 7	23	A8	D5 15	BIB 2
ADD 8	1	A7	D4 14	BIB 3
ADD 9	2	A6	D3 13	BIB 4
ADD 1Ø	3	A5	D2 11	BIB 5
ADD 11	4	A4	D1 1Ø	BIB 6
ADD 12	5	A3	DØ 9	BIB 7
ADD 13	6	A2		
ADD 14	7	A1		
ADD 15	8	AØ		

U23 28S166

LOAD+ 18 → G3, 19 → G2
BSTRBD– 20 → GT

ADD 5	21	A1Ø	D7 17	BIB 8
ADD 6	22	A9	D6 16	BIB 9
ADD 7	23	A8	D5 15	BIB 1Ø
ADD 8	1	A7	D4 14	BIB 11
ADD 9	2	A6	D3 13	BIB 12
ADD 1Ø	3	A5	D2 11	BIB 13
ADD 11	4	A4	D1 1Ø	BIB 14
ADD 12	5	A3	DØ 9	BIB 15
ADD 13	6	A2		
ADD 14	7	A1		
ADD 15	8	AØ		

2/ 3/ 16/ 16/

DATA 15	J3-31
DATA 14	J3-29
DATA 13	J3-27
DATA 12	J3-25
DATA 11	J3-23
DATA 1Ø	J3-21
DATA 9	J3-19
DATA 8	J3-17
DATA 7	J3-15
DATA 6	J3-13
DATA 5	J3-11
DATA 4	J3-9
DATA 3	J3-7
DATA 2	J3-5
DATA 1	J3-3
DATA Ø	J3-1
ADD 15	J3-32
ADD 14	J3-3Ø
ADD 13	J3-28
ADD 12	J3-26
ADD 11	J3-24
ADD 1Ø	J3-22
ADD 9	J3-2Ø
ADD 8	J3-18
ADD 7	J3-16
ADD 6	J3-14
ADD 5	J3-12
ADD 4	J3-1Ø
ADD 3	J3-8
ADD 2	J3-6
ADD 1	J3-4
ADD Ø	J3-2
DXW–	J3-38
DXR–	J3-36
DXFETCH–	J3-34
BRESET–	J3-37

J3-4Ø, J3-42

ITEM OR FIND NO.	QTY REQD	NOMENCLATURE OR DESCRIPTION	MATL SPEC AND SIZE OR COMPONENT VALUE	IDENTIFYING OR PART NO.	CODE IDENT.

PARTS LIST

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMAL ±
FRACTIONS ± ANGLES ± 0° 30'
MAX SURFACE ROUGHNESS 125 ALL MACHINED SURFACES EXCEPT AS NOTED
BREAK SHARP EDGES AND CORNERS .010 MAX
FINISH

CONTRACT NO.

DWN S. ABEL 21 DEC 82
ENGR J. PARISH
CHK [redacted] 83
PROD
APVD
APVD

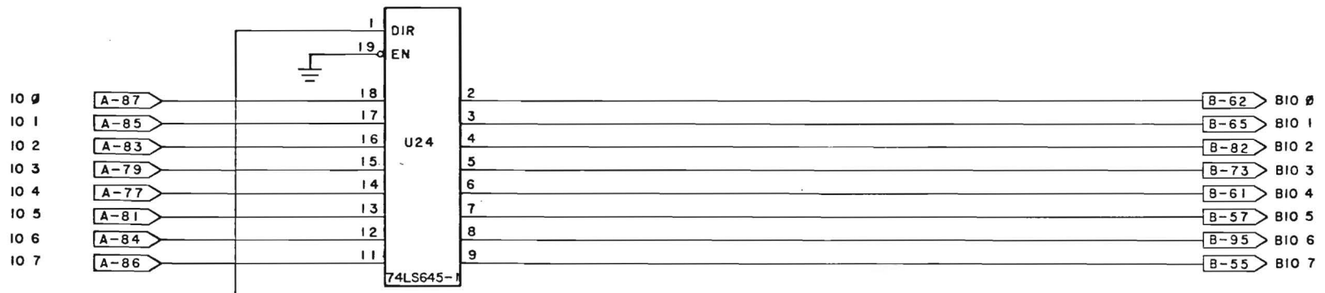
ENGINEERING EXPERIMENT STATION OF THE GEORGIA INSTITUTE OF TECHNOLOGY ATLANTA GEORGIA

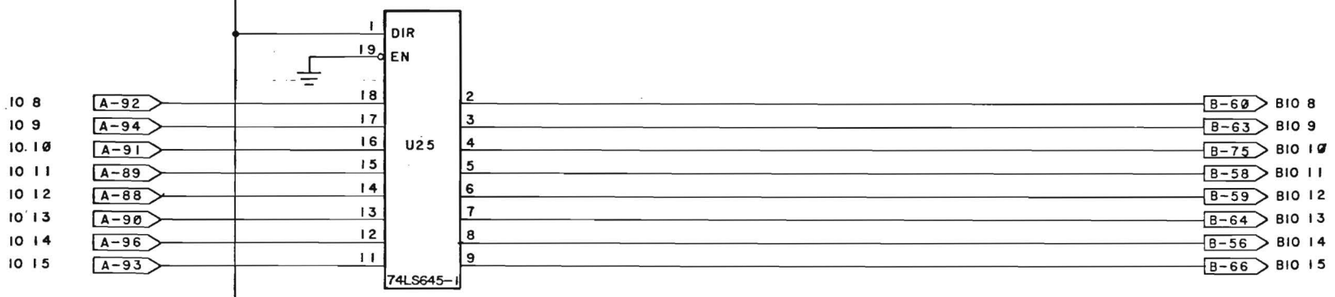
SCHEMATIC DIAGRAM EEPROM CPU ADAPTER APL CIRCUITRY

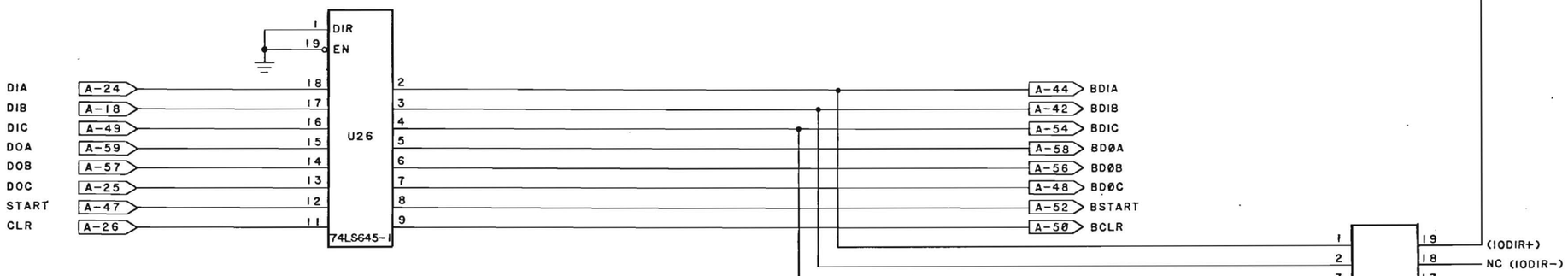
SIZE D | CODE IDENT. NO. 07101 | DRAWING NO. A3183-011-E4 | REV

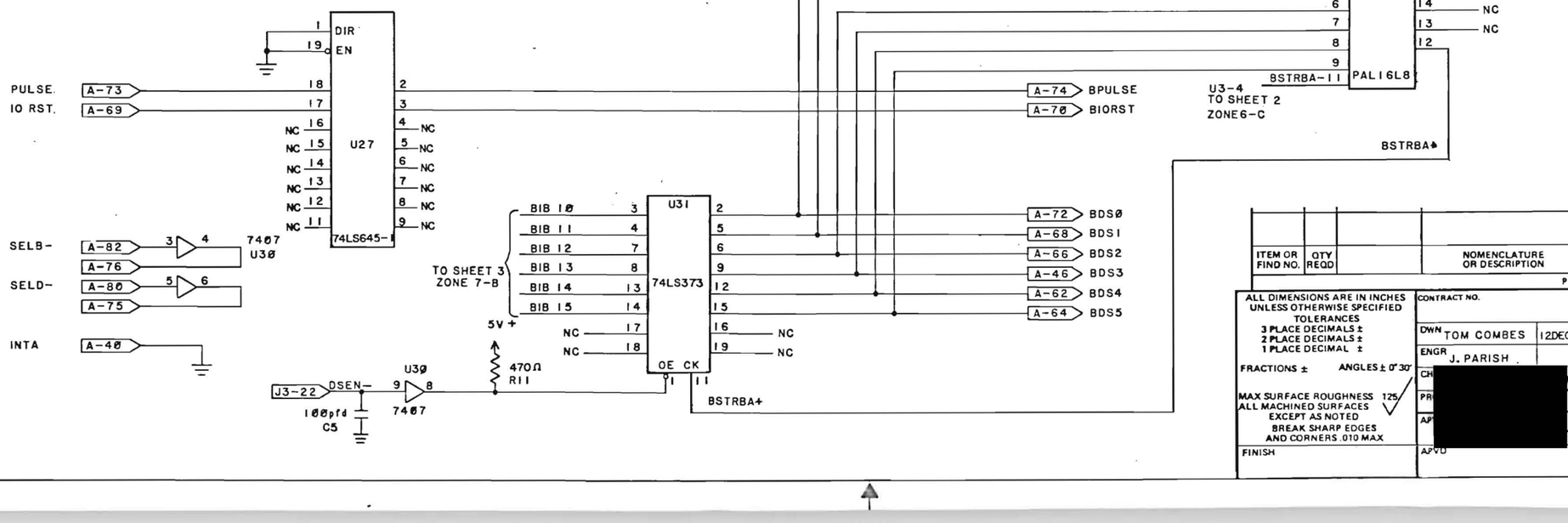
SCALE N.T.S. | SHEET

APPLICATION			REVISIONS				
QTY REQD	NEXT ASSY	USED ON	ZONE	SYM	DESCRIPTION	DATE	APPROVED









ITEM OR FIND NO.	QTY REQD	NOMENCLATURE OR DESCRIPTION	MATL SPEC AND SIZE OR COMPONENT VALUE	IDENTIFYING OR PART NO.	CODE IDENT.

PARTS LIST

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMAL ±
FRACTIONS ± ANGLES ± 0°30'
MAX SURFACE ROUGHNESS 125
ALL MACHINED SURFACES EXCEPT AS NOTED
BREAK SHARP EDGES AND CORNERS .010 MAX
FINISH

CONTRACT NO.

DWN TOM COMBES 12DEC82
ENGR J. PARISH
CH [redacted] /83
PR
AP
APVD

ENGINEERING EXPERIMENT STATION OF THE GEORGIA INSTITUTE OF TECHNOLOGY ATLANTA, GEORGIA

SCHEMATIC DIAGRAM EEPROM CPU ADAPTER I/O BUS BUFFER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	07101	A3183-011-E4	

SCALE NTS SHEET 5 OF 5